Academic Program: PG

Academic Year 2025-26

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

III & IV Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

Ph: 0836-2447465 **Fax: 0836-2464638** **Web: www.sdmcet.ac.in**

SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for III & IV semester M.Tech in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2025-26 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION

To develop competent professionals with human values.

MISSION

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives(PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self-confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and lifelong learning in the broadest context of technological changes.

Scheme for III Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
24PDEC300	Advances in VLSI Design	4-0-0	4	50	100	3		
24PDEE35X	Elective 5	4-0-0	4	50	100	3		
24PDEE35X	Elective 6	4-0-0	4	50	100	3		
24PDEE35X	Elective 7	4-0-0	4	50	100	3	--	--
OR								
24PDEL300	**Internship in Industry or R&D organization	Min 4 weeks during vacation after 2nd sem	4	50	--	--	100	3
24PDEL301	***Project Phase-I	0-0-6	6	50	--	--	50	3
Total		**16-0-6/12-4weeks-6**	**22**	**250**	**400/ 300**		**50/150**	

Course Code	Course Title
24PDEE350	Real Time Operating Systems
24PDEE351	Error Control Coding
24PDEE352	Wireless Sensor Networks
24PDEE353	Data Compression
24PDEE354	Deep Learning
24PDEE355	Computer Vision
24PDEE356	Digital Circuit Testing & Testability
24PDEE357	Analog and Mixed Mode VLSI Circuits

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

***SEE** for theory courses is conducted for 100 marks and reduced to 50 marks.

****Internship**: The students are expected to undergo training in industry for a period of ***four weeks*** during the vacation immediately after completion of II Semester examination. A faculty is to be allotted to guide the student. A committee consisting of three faculty members shall evaluate the work carried out and the knowledge the students have acquired. **OR students can take one elective course if they do not undergo internship.**

*****Project Phase-I: The students are expected to formulate the problem and carry out the intensive literature survey along with preliminary investigations supporting the project phase-II in IV semester.

Scheme for IV Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
24PDEL400	**Project Phase-II	0-0-22	18	100	--	--	100	3
24PDEEOA1	***BOS recommended ONLINE course	-	Audit (PP)	-	-	-	-	-
24PDEEOA2	***BOS recommended ONLINE course	-	Audit (PP)	-	-	-	-	-
Total		**0-0-22**	**18**	**100**	**--**	**--**	**100**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

- SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

** Project Phase-II: The students are expected to work on a project for the full semester in an industry or an institution

*** Classes and evaluation procedures are as per the policy prescribed for online courses by the institution.

Total Credits offered for the first year: 40
Total Credits offered for the Second year: 40

III Semester

24PDEC300	Advances in VLSI Design	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on Implementation strategies for digital ICS from custom to semicustom Array Design. The performance parameters of CMOS circuits and timing issues of digital system are addressed. The Memory design and array structure are implemented using Programmable logic device (PLD).

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Apply** design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.	-	1,3	-
CO-2	**Use** the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability	1,5	-	-
CO-3	**Impose** the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.	1,3	5	6
CO-4	**Infer** the reliability of the memory	-	1,6	-
CO-5	**Understand** the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories	1	2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.6	1	2.5	-	2.5	1.5

Pre-requisites: Digital VLSI Design, ASIC Design

Contents:

1) **Implementation Strategies For Digital ICS:** Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future. **10 Hrs**

2) **Coping With Interconnect:** Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability- Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques,Reduced Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip**.** **10 Hrs**

3) **Timing Issues In Digital Circuits:** Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock Distribution Techniques, Latch-Base Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self- Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. **11 Hrs**

4) **Super Buffers, Bi-CMOS, Steering Logic & Special circuits:** Introduction, RC delay lines, super buffers, An NMOS super buffer, tri state super bufer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic., General functional blocks-NMOS & CMOS functional blocks. Tally circuits, NAND-NAND, NOR-NOR & AOI logic, Multiplexers & Barallel Shifters. **11 Hrs**

5) **Issues of Designing Memory and Array Structures:** Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions. **10 Hrs**

Reference Books:

1) Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits-A Design Perspective”, PHI, 2ndEdition, 2003.

2) M. Smith, “Application Specific Integrated circuits”, Addison Wesley, 1997.

3) Wang, Wu and Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann, 2006.

4) H. Veendrick, “MOS ICs: From Basics to ASICs”, Wiley-VCH, 1992.

5) Eugene D. Fabricius, "Introdution to VLSI Design", McGraw Hill International Publications-1990.

24PDEE350	Real Time Operating Systems	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on concepts of real-time systems, computing required for the real-time embedded systems and communication required for the real-time embedded systems.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the concept of mathematical model of the system.	3	-	1
CO-2	**Describe** real-time algorithm for task scheduling.	-	3,4	2
CO-3	**Understand** the working of real-time operating systems	1	-	5,6
CO-4	**Analyze** working of real-time database	-	4	5
CO-5	**Describe** the design and development of protocols related to real-time communication	-	5	4

POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
Mapping Level	2	1	2.5	2	1.5

Pre-requisites: Operating systems, Embedded systems

Contents:

1) **Introduction:** Introduction to real time systems, Application of real time systems, Basic model of real time systems, characteristics of real time systems, safety and reliability, types of real time tasks, Timing Constraints, Modeling timing constraints. **06 Hrs**

2) **Real Time Task Scheduling:** Some important concepts, Types of real time tasks and their characteristics, task scheduling, clock-driven scheduling, Hybrid schedulers, Event-driven scheduling, Earliest Deadline first scheduling, rate Monotonic algorithm, some issues associated with RMA, issues in using RMA in practical situations. **08 Hrs**

3) **Handling resource sharing and dependencies among real time task:** Resource sharing among real time tasks, Priority inversion, priority inheritance protocol, highest locker protocol, priority ceiling protocol, different types of priority inversion under PCP, important features of PCP, some issues in using a resource sharing protocol, handling task dependencies. **08 Hrs**

4) **Scheduling Real-time tasks in multiprocessor and Distributed systems:** Multiprocessor task allocation, Dynamic allocation of tasks, fault-tolerance scheduling of task, clock in distributed real-time systems, centralized clock synchronization, distributed clock synchronization. **08 Hrs**

5) **Commercial Real-time operating systems:** time services, features of real time operating systems, Unix as a real time operating systems, Unix-based real time operating systems, Windows as a real time operating systems, Portable operating system interface, a survey of contemporary real time operating systems, Benchmarking Real time systems . **08 Hrs**

6) **Real time communications:** examples of real time communication in applications, Basic concepts, Real time communication in LAN, soft real time communication in a LAN, Hard real time communication in a LAN, Bounded Access protocol, performance comparison, real-time communication over internet, Routing Multicast routing, resource reservation, Traffic shaping and policing, Scheduling Mechanism, QoS Models. **08 Hrs**

7) **Real time Databases:** Review of basic database systems, Realtime databases, Characteristics of Temporal data, Concurrency Control in Realtime databases, Commercial Real-time databases. **06 Hrs**

Reference Books:

1) Rajib Mall, Real-Time Systems: Theory and Practice, Pearson Education, 2007

2) C. Siva Ram Murthy and G. Manimaran, 'Resource Management in Real Time Systems and Networks', the MIT Press, 2001

3) C. Mani Krishna, Kang G. Shin, Publisher McGraw-Hill, 1997

24PDEE351	Error Control Coding	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on understanding the principles of error detection and correction, applying coding techniques, and analyzing the performance of different coding schemes.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design and Analyze** Linear block codes.	-	1,4,5	-
CO-2	**Design and Analyze** Cyclic codes	-	1,4,5	-
CO-3	**Explain and analyze** BCH Codes and Majority Logic Decodable Codes.	-	1,4	-
CO-4	**Design and Analyze** Convolution Codes.	-	1,4,5	-
CO-5	**Explain and analyze** Concatenated Codes & Turbo Codes	-	1,4	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	-	-	2	2	-

Pre-requisites: Information Theory & coding, Digital Communication

Contents:

1) **Linear Block Codes:** Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Hamming Codes, Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes. **12 Hrs**

2) **Cyclic Codes:** Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes – Encoding using Feedback shift register circuits, Generator matrix for Cyclic codes, Syndrome

computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, (23, 12) Golay code, Shortened cyclic codes. **10 Hrs**

3) **BCH Codes and Majority Logic Decodable Codes :** Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Reed – Solomon Codes, One – Step Majority logic decoding, one – step Majority logic decodable Codes. **10 Hrs**

4) **Convolution Codes:** Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Stack and Fano sequential decoding Algorithms. **10 Hrs**

5) **Concatenated Codes & Turbo Codes:** Single level Concatenated codes, Multilevel Concatenated codes, Turbo coding and their distance properties, LDPC Coding. **10 Hrs**

Activity beyond Syllabus: Assignments on the design of various coding techniques.

Reference Books:

1) Shu Lin & Daniel J. Costello, Jr. “Error Control Coding”, Pearson Education India, 2010.
2) Blahut R. E R.E., “Theory and Practice of Error Control Codes”, Addison Wesley, 1984.
3) Satyanarayana P.S., “Concepts of Information Theory & coding”, Dynaram Publications, Bangalore, 2005.
4) Ranjan Bose, “Information Theory, Coding and Cryptography”, Tata McGraw-Hill Publication, 2002.

24PDEE352	Wireless Sensor Networks	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on architecture of Wireless sensor nodes, Operating systems used in WSN, Medium Access Control Protocols, Networks Protocols, Power Management, Time Synchronization, Localization and security issues in WSN.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** various parts of WSN and **explain** their construction and operation.	3	-	-
CO-2	**Apply** suitable medium access control technique for a given application of WSN.	3	1	-
CO-3	**Apply** suitable data dissemination and routing protocol for a given application of WSN.	4	5	1
CO-4	**Apply** various techniques and **solve** the problems related to power efficiency and synchronization in WSN.	-	4	1
CO-5	**Apply** the techniques and **determine** solutions various issues related to localization and security issues in WSN.	-	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.33	-	3	2.4	2	1

Pre-requisites: Sensors and Actuators, Wireless Communication, Microcontrollers, Communication Network protocols.

Contents:

1) **Wireless Sensor Network Basics**: Motivation, Definitions and Background, Challenges and Constraints, Areas of Applications, Node Architecture, Sensing

Subsystem, Processor Subsystem, Communication Interfaces, Operating Systems, Functional and Non functional aspects of OS. **08 Hrs**

2) **Medium Access Control:** Medium Access Control, Overview, Wireless MAC Protocols, Characteristics of MAC Protocols in Sensor Networks, Contention-Free MAC protocols, Contention based MAC protocols, Hybrid MAC protocols. **10 Hrs**
3) **Network Layer**: Overview, Routing Metrics, Flooding and Gossiping, Data-centric Routing, Proactive Routing, On-Demand Routing, Hierarchical Routing, Location based Routing, QoS based routing protocols. **10 Hrs**

4) **Power Management and Time Synchronization:** Local Power Management Aspects, Dynamic Power Management, Conceptual Architecture, Clocks and synchronization problem, Time synchronization in WSN, Basics of Time synchronization, Time synchronization protocols. **12 Hrs**

5) **Localization and Security:** Overview, Ranging Techniques, Range based Localization, Range-Free Localization, Event Driven Localization, Fundamentals of Network Security, Challenges of Security in WSN, Security Attacks in Sensor Networks, Protocols and Mechanisms for Security. **12 Hrs**

Reference Books:

1) Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks”, Wiley Publications, 2014.
2) Kazem Sohraby, Daniel Minoli, Taieb Znati “Wireless Sensor Networks”, Wiley Publications, 2015.
3) Jun Zeng, Abbas Jamalipour "Wireless Sensor Networks", Wiley Publications, 2014.
4) S. Swapnakumar, "A Guide to Wireless Sensor Networks”, Laxmi Publications, 2013.

22PDEE353	Data Compression	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the need for compression, various lossless and lossy compression techniques and their performance measures. Some of the standards recommended for speech and video coding are also explained.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** various compression techniques and **understand** the principles of different types of quantization	-	4	-
CO-2	**Analyze** various differential encoding methods	-	4	-
CO-3	**Analyze** various transform coding methods	4	3,5	-
CO-4	**Apply** analysis/ synthesis schemes for speech compression.	4	1,5	-
CO-5	**Understand** various speech, image and video compression standards.	-	1,5	-
CO-6	**Design and compare** various lossless coding methods.	4	1,5	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	-	2	2.6	2	-

Pre-requisites: Digital Signal Processing, Digital Communication, Information Theory and Coding.

Contents:

1) **Introduction:** Compression techniques, Modeling & coding, Distortion criteria. **04 Hrs**

2) **Quantization:** Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Trellis coded quantization. **08 Hrs**

3) **Differential Encoding:** Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation. **06 Hrs**

4) **Transform Coding:** Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression. **07 Hrs**

5) **Analysis/Synthesis Schemes:** Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression. **07 Hrs**

6) **Video Compression:** Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video. **08 Hrs**

7) **Lossless Coding:** Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Dictionary techniques – LZ77, LZ78, Applications of LZ78 – JBIG, JBIG2, Predictive coding – Prediction with partial match, Burrows Wheeler Transform, Applications – CALIC, JPEG-LS. **12 Hrs**

Reference Books:

1) K. Sayood, “Introduction to Data Compression," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.
2) N. Jayant and P. Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video,” Prentice Hall, USA, 1984.
3) D. Salomon, “Data Compression: The Complete Reference”, Springer, 2000.
4) Z. Li and M.S. Drew**,** “Fundamentals of Multimedia,” Pearson Education, 2004.

24PDEE354	Deep Learning	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course deals with the basics of deep learning. It is aimed at understand the working of Convolutional Neural Networks and RNN in decision making. The course also illustrates the strength and weaknesses of many popular deep learning approaches. It introduces major deep learning algorithms, the problem settings, and their applications to solve real world problems.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** various concepts of neural networks, relationship between perceptron and classifiers.	1, 5	-	-
CO-2	**Understand and Implement** the multilayer perceptrons and back-propagation algorithm.	-	2	6
CO-3	**Realize and Implement** semi-supervised learning, and perform neural network optimization.	3, 5	-	6
CO-4	**Implement** the algorithms using convolutional neural networks.	1, 4	2	-
CO-5	**Understand and Implement** the recurrent and recursive nets, LSTM.	4	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	2.0	1.8	-	1.0	-

Pre-requisites: Linear Algebra, basics of probability.

Contents:

1) **Introduction:** What is a Neural Network?, The Human Brain, Models of a Neuron, Neural Networks Viewed As Directed Graphs, Feedback, Network

Architectures, Rosenblatt‟s Perceptron: Introduction, Perceptron,The Perceptron Convergence Theorem, Relation Between the Perceptron and Bayes Classifier for a Gaussian Environment. **10 Hrs**

2) **Multilayer Perceptrons:** Introduction, Batch Learning and On-Line Learning, The Back-Propagation Algorithm, XOR Problem, Heuristics for Making the Back- Propagation Algorithm Perform Better, Back Propagation and Differentiation. **10 Hrs**

3) **Regularization for Deep Learning:** Parameter Norm Penalties - L2 Parameter Regularization, Dataset Augmentation, Semi-Supervised Learning. Optimization for Training Deep Models: Challenges in Neural Network Optimization – Ill Conditioning, Local Minima, Plateaus, Saddle Points and Other Flat Regions. **10 Hrs**

4) **Convolution neural networks:** The Convolution Operation, Motivation, Pooling, Convolution and Pooling as an Infinitely Strong Prior, Variants of the Basic Convolution Function, Structured Outputs, Data Types, Efficient Convolution Algorithms, Convolutional Networks and the History of Deep Learning. **10 Hrs**

5) **Sequence Modeling:** Recurrent and Recursive Nets: Unfolding Computational Graphs, Recurrent Neural Networks, Bidirectional RNNs, Encoder-Decoder Sequence-to- Sequence Architectures, Deep Recurrent Networks, Recursive Neural Networks, The Long Short-Term Memory and Other Gated RNNs. **12 Hrs**

Reference Books:

1) Simon Haykin, Neural networks and Learning Machines, Third Edition, Pearson, 2016.
2) Ian Goodfellow, Yoshua Bengio and Aaron Courville, Deep Learning, MIT Press, 2016. https://www.deeplearningbook.org/lecture_slides.html.
3) Francois Chollet, Deep Learning with Python, Manning Publications, 2017, ISBN10, 9781617294433.
4) Aston Zhang, Zachary C. Lipton, Mu Li, and Alexander J. Smola,Dive into Deep Learning Release 0.8.0, 2020.
5) C. M. Bishop, Pattern Recognition and Machine Learning (Information Science and Statistics),Springer, 2006.

24PDEE355	Computer Vision	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

Students will learn basic principles of image formation, imaging geometry, image processing algorithms and various algorithms and methods involved for computer vision. This course also emphasizes the core vision tasks of scene understanding and recognition,motion estimation, object recognition and various vision-based applications such as face recognition, surveillance, human gait analysis etc. to name a few.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Understand** fundamentals of computer vision and its applications	-	2	1
CO-2	**Apply** suitable image enhancement and restoration techniques.	-	2, 3	1,5
CO-3	**Acquire** knowledgeand **apply** image segmentation and feature extraction methods on given image	-	2,3	1,5
CO-4	**Apply** the motion concepts and its relevance in real time applications	3	2	1,5
CO-5	**Implement** various object detection and Recognition algorithms on available online image datasets	3	2	1,5
CO-6	**Apply** the knowledge in solving high level vision problems like object recognition, image classification etc	3	2	1,5

POs/PSOs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	2.0	2.6		1.0	

Pre-requisites Calculus, Linear algebra, Probability, Programming knowledge

Contents:

1) **Introduction to computer vision:** Overview of computer vision and its applications, Image Formation and Representation: Imaging geometry, radiometry, digitization, cameras and Projections, rigid and affine transformation. **10 Hrs**

2) **Image representation & Analysis**: Image representation, Image processing techniques like color and geometric transforms, Edge-detection techniques, Filtering, Mathematical operations on image and its applications like convolution, filtering. **08 Hrs**

3) **Feature Extraction:** Importance of Features, Feature extraction techniques, Histogram of Oriented Gradient (HOG), Scale Invariant Feature Transform (SIFT), Background subtraction techniques, Image Matching, Principal Component Analysis (PCA) **08 Hrs**

4) **Motion estimation**: Introduction to motion, Regularization theory, Optical computation, Stereo Vision, Motion estimation, Structure from motion and models. **08 Hrs**

5) **Object recognition:** Hough transforms and other simple object recognition methods, Shape correspondence and shape matching, Shape priors for recognition, Object Recognition techniques: Viola-Jones, Yolo. **08 Hrs**

6) **Applications**: Photo album, Face detection, Face recognition, Eigen faces, Active appearance and 3D shape models of faces Application: Surveillance, foreground background separation, tracking, and occlusion, combining views from multiple cameras, human gait analysis. **10 Hrs**

Activity beyond Syllabus: Seminar, Simulation based Project

Reference Books:

1) R. Szeliski, “Computer Vision: Algorithms and Applications”, 1st edition, Springer, 2011.
2) D. Forsyth and J. Ponce, “Computer Vision - A modern approach”, 2nd edition,Prentice Hall, 2011.
3) E. Trucco and A. Verri, “Introductory Techniques for 3D Computer Vision”,Publisher: Prentice Hall, 1998
4) R. C. Gonzalez and R. E. Woods, “Digital Image Processing”, 2nd edition, Pearson Education (Asia) Pvt. Ltd, Prentice Hall of India, 2004.

24PDEE356 Digital Circuit Testing & Testability (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the design & testability aspects of combinational & sequential circuits. Also address the design & testability issues with built in test circuits, memory units and self checking circuits. It demonstrates various test algorithms for different digital circuits at various levels of design.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	Describe the Testability of Combinational Circuits.	-	3,4	-
CO-2	Explain the Testability of Sequential Circuits.		3,5	-
CO-3	Illustrate the concepts of Built In Self-Test.	2	-	-
CO-4	Demonstrate the design for Testability of Memory Circuits.	1,6	-	-
CO-5	Illustrate Self Checking Circuits using various techniques.	1,6	-	-

POs/PSOs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3	3	2	2	2	3

Pre-requisites: Digital Circuits, Digital VLSI Design

Contents:

1) **Design for Testability for Combinational Circuits** Stuck at Faults, Fault diagnosis by Path Sensitization Technique, Reed Muller's expansion technique, OR-AND-OR design, Automatic Synthesis of Testable Logic, Testable design of Multilevel Combinational Circuits. **10 Hrs**

2) **Design for Testability for Sequential Circuits** Controllability and observability, Ad-Hoc Design Rules for Improving Testability, Scan Path Technique for testable Sequential Circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, partial Scan, Boundary Scan. **10 Hrs**

3) **Built-In Self-Test** Test Pattern generation for BIST, Output Response Analysis, Circular BIST, Built-In logic Block observer, Self-Testing using an MISR and Parallel Shift register Sequence generator, LSSD On-Chip Self-Test. **10 Hrs**

4) **Testable Memory Design** RAM fault Models, Test Algorithms for RAMs-Galloping 0's and 1's,Walking 0's and 1's, March Test, MATS Check Board Test, Detection of Pattern-Sensitive Faults, BIST Techniques for RAM Chips. **10 Hrs**

5) **Self - Checking Circuits** Basic concepts of Self checking circuits, Design of Totally Self Checking checker- Self Checking using m/n codes, Equality Checkers, Berger code, Self-Checking Combinational Circuits, Self - Checking Sequential Circuit. **12 Hrs**

Reference Books:

1) Parag K. Lala, "An Introduction to Logic Circuit Testing", Morgan & Claypool Publishers, 2009.
2) Parag K. Lala, Digital Circuit Testing and Testability, Academic Press, 1997.
3) Miron Abramovici, M.A. Breues, A. D. Friedman, "Digital Systems Testing and Testable Design", Jaico publications, 2001.
4) Zainalabedin Navabi, "Digital System Test and Testable Design: Using HDL Models and Architectures", Springer, 2011.

24PDEE357 Analog and Mixed Mode VLSI Circuits (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the basic requirements of circuit design, diffulties in the design phase and various circuit examples. The course considers widely used analog circuits such as differential amplifiers, Current mirrors, OPAPM, ADC, DAC and PLL as examples for the discussion.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	Explain basic physics and operation of MOS devices.	-	3,4	-
CO-2	**Analyze** and Design various configuration (CS, CD, CG) of Single stage amplifiers.	5	-	-

CO-3	**Design** the analog circuits such as differential amplifiers, current sinks and sources and Op amps.	5	-	-
CO-4	**Design** and **study** the behavior of phase-locked-loops for the applications.	5,6	-	-
CO-5	**Perform** calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.	6	-	-

POs/PSOs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	-	2	2	3	3

Pre-requisites: CMOS VLSI Design, Network Theory.

Contents:

1) **Basic MOS Device Physics**: General considerations, MOS I/V Characteristics, second order effects, MOS device models.
   Single stage Amplifier: Basic Concepts, Common Source stage. **10 Hrs**

2) **Other single stage amplifiers:** Source follower, common-gate stage, Cascode Stage, choice of device models.
   Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. **10 Hrs**

3) **Analog CMOS Sub-circuits**: MOS Switch, Current sinks and sources, Current mirrors.
   Operational Amplifiers: General Considerations, One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection**.** **10 Hrs**

4) **Phase Locked Loops**: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications. **10 Hrs**
5) **Data Converter Architectures**: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. **12 Hrs**

Reference Books:

1) Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2008.

2) R. Jacob Baker, Harry W. LI, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 2005.

3) Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press, 2011.

24PDEL300 Internship (4 weeks) 4

Course Learning Objectives (CLOs):

The curriculum has the support for internship to be carried out during vacation immediately after the completion of II semester examination for a minimum period of four weeks in any of the reputed Industries/ Academic Institutes/ R&D Organizations. Students may identify the Industries considering their career choice. The objectives are:

- Internships are intended to provide students with an opportunity to apply theoretical concepts from the classroom to the realities of the field.
- Will expose students to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.
- Provides exposure to the current technological developments relevant to the subject area of training.
- Provides an opportunity to explore and develop their careers through professional practice. Helps students to communicate in a workplace environment in a clear and confident manner and articulate their experience and skills to potential employers.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Acquire** practical experience in an organizational setting	-	1,6	-
CO-2	**Apply** the knowledge and skill set in engineering design processes appropriate to the	1,4	3,5	-

	internship program			
CO-3	**Apply** modern tools and processes to solve the live problems	-	4	-
CO-4	**Get** an opportunity to learn new skills	-	5	-
CO-5	**Learn** strategies like time management, multi-tasking, communication and team work skills in an industrial setup.	-	2,5,6	-

POs	1	2	3	4	5	6
Mapping levels	2.5	2	2	2.5	2	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field and explore solutions. They are required to know the functions of engineers in managing the floor. Current technological developments, organizational behavior, time management, professional ethics, etc. need to be understood.

2) The above skills obtained need to be documented and presented.

Reference Material:

1) Technical references/research papers
2) Manuals
3) Software packages

24PDEL301 Project Phase - I (0-0-6) 6

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote independent learning. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** innovative/research based problem statement through literature survey	1,4,5	-	-
CO-2	**Explore** and **analyze** possible technical solutions for the problem identified	4,5	-	-
CO-3	**Demonstrate** the work progress	3	-	-
CO-4	**Prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in the previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field through literature survey and select a topic from emerging area relevant to the branch.

2) The students are expected to explore and analyze all possible technical solutions for the problem identified and start working on the same using tools.Preliminary design, analysis, simulation etc. is to be done in this phase.

3) The students are expected to document the work done in a systematic way and learn/improve the presentation skills.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools

IV semester

24PDEL400 Project Phase - II (0-0-22) 18

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote team work. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Design** and **Implement** the solution	1,4,5	-	-
CO-2	**Discuss** the outcome of the work	3,4,5	-	-
CO-3	**Justify** the approach and **Integrate** the work carried out by producing technical paper	2,3	-	-
CO-4	**Organize** the topics in a systematic manner and **prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to continue the work providing feasible solutions, justify the approach, defend the same and present the work in national / international conferences or journals.

2) The students are expected to document the work done in a systematic way and deliver the oral presentation.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools