Academic Program: PG

Academic Year 2025-26

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

I & II Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for I & II semester M.Tech. in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering &Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2025-26 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION:

To develop competent professionals with human values.

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state-of-the-art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives (PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self-confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and life long learning in the broadest context of technological changes.

Scheme for I Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
24PDEC100	Applied Mathematics	3-0-0	3	50	100	3	-	-
24PDEC101	Digital System Design Using Verilog	3-0-0	3	50	100	3	-	-
24PDEC102	Sequential Machines and Fault Analysis	3-0-0	3	50	100	3	-	-
24PDEC103	Digital VLSI Design	3-0-0	3	50	100	3	-	-
24PDEC104	Nano Electronics	3-0-0	3	50	100	3	-	-
24PRMC105	Research Methodology and IPR	2-0-0	2	50	100	3	-	-
24PDEL101	Digital Circuits Simulation Laboratory	0-0-2	1	50	-	-	50	3
Total		**17-0-2**	**18**	**350**	**600**		**50**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

- SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

Scheme for II Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
24PDEC200	VLSI for Signal Processing	4-0-0	4	50	100	3	-	-
24PDEC201	Advanced Embedded Systems	4-0-0	4	50	100	3	-	-
24PDEE25X	Elective 1	4-0-0	4	50	100	3	-	-
24PDEE25X	Elective 2	4-0-0	4	50	100	3	-	-
24PDEE25X	Elective 3	4-0-0	4	50	100	3	-	-
24PDEL201	Advanced Embedded Systems Laboratory	0-0-2	1	50	-	-	50	3
24PDEC202	Seminar	0-0-2	1	50	-	-	-	-
Total		**20-0-4**	**22**	**350**	**500**		**100**	

Electives 1 to 3

24PDEE250	Advanced Computer Architecture
24PDEE251	Low Power Circuits and Systems
24PDEE252	Artificial Intelligence and Machine Learning
24PDEE253	Image and Video Processing
24PDEE255	Cryptography and Network Security
24PDEE256	5G Wireless Communication

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

- SEE for theory courses is conducted for **100 marks** and reduced to **50 marks**.
- Seminar is to be conducted every week and 2-3 students/week will present a topic from emerging areas in respective PG program preferably the contents not studied in their regular courses. The seminar shall be evaluated by 2 faculty members having specialization in respective program and allied areas.

I semester

24PDEC100	Applied Mathematics	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs): This course will enable students to acquaint with principles of Probability theory, Random process, Linear Algebra, Wavelet transforms, Laplace transform and Linear programming problems and apply the knowledge in the applications of Electronics and Communication Engineering Sciences.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Learn the idea of random variables (discrete/continuous) and probability distributions in analysing the probability models arising in random processes.	-	1,2	-
CO-2	Learn the concept of Wavelets and its Applications to Denoising	-	1,2	-
CO-3	Apply Linear Algebra, QR and singular value decomposition techniques for data compression, least square approximation in solving inconsistent linear systems.	-	1,2	-
CO-4	Apply transform method to solve one-dimensional wave equation, one-dimensional heat equation, Laplace equation, Poisson equation.	-	1,2	-
CO-5	Solve system of linear and non-linear equation arising in engineering fields	-	1,2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	2.0	-	-	-	-

Pre-requisites: Basics of Probability, Differentiation and Integration, Vectors.

Contents:

1) **Probability Theory:** Review of basic probability theory, Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions and examples. **08 Hrs**
2) **Introduction to Wavelets:** Introduction, The origin of wavelets, wavelets and other reality transforms, Wavelets in future, Continuous Wavelets: First level of introduction of wavelet transforms, Continuous time frequency representation of signals, Discrete Wavelet Transform signal decomposition (Analysis) frequency response, signal reconstruction. Applications of Wavelets in science and Engineering.

   Denoising: Introduction, Denoising using wavelet shrinkage – statistical modelling and estimation, Noise estimation, Denoising Images with MATLAB. **08 Hrs**
3) **Linear Algebra:** Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method, Orthogonal vectors and orthogonal bases, Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations**.** **07 Hrs**
4) **Transform Methods:** Laplace transform methods for one dimensional wave equation – Applications, Fourier transform methods for one dimensional heat equations and applications, Fourier transform methods for Laplace equation and Poisson equation, problems. **08 Hrs**
5) **Linear and Nonlinear Programming:** Simplex Algorithm and simplex method, Nonlinear Programming–Constrained extremal problems: Lagranges multiplier method, Kuhn-Tucker conditions and solutions. **08 Hrs**

Reference Books:

1) Richard Bronson*, "*Schaum's Outlines of Theory and Problems of Matrix Operations"*,* McGraw-Hill, 1988.
2) Venkataraman M K, "Higher Engineering Mathematics", National Pub.Co,1992.
3) Sneddon, I. N., "Elements of partial differential equations", Dover Publications, 2006.
4) Taha H A, "Operations research- An Introduction", Mc Milan Publishing Co, 1982.
5) K. P. Soman, K.I. Ramachandran, G. Resmi, "Insight into Wavelets (From theory to Practice)", PHI Publications, 3rd edition. 2010.

24PDEC101 Digital System Design using Verilog (3-0-0)3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on design of various combinational and sequential circuits and design methodology. It also discusses the implementation of advanced digital circuits on programmable devices of varied complexity.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the basic concepts of digital system design using Verilog.	-	4	-
CO-2	**Design** the real-life applications using Verilog.	4	5	1
CO-3	**Design** and **Model** various sequential circuits and memories using Verilog.	4	5	-
CO-4	**Describe** various programmable Logic Devices.	-	5	-
CO-5	**Design** processors and controllers using Verilog, for embedded applications.	5	-	6
CO-6	**Elaborate** different I/O devices and fault modeling techniques.	-	-	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	-	2.66	2.25	1

Pre-requisites: Digital Circuit Design, HDL Programming using verilog

Contents:

1) **Introduction and Methodology**: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **08 Hrs**
2) **Sequential Basics**: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology. **08 Hrs**
3) **Memories**: Concepts, Memory Types, Error Detection and Correction. **05 Hrs**

4) **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **05 Hrs**
5) **Processor Basics**: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **04 Hrs**
6) **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **05 Hrs**
7) **Design Methodology**: Design flow, Design optimization, Design for test. **04 Hrs**

Reference Books:

1) Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using Verilog", Elsevier, 2010.
2) Charles H. Roth, Jr., LizyKurian John, ByeongKil Lee, "Digital Systems Design Using Verilog", 1/e, Cingage Learning, 2014.
3) Samir Palnitkar, "Verilog HDL", 2/e, Pearson Education, 2015.
4) Nazeih M Botros, "HDL Programming, VHDL and Verilog", Dreamtech Press, 2007.

24PDEC102 Sequential Machines and Fault analysis (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on threshold logic, fault detection and location in combinational circuits. It also covers the detailed sequential machine minimization procedures, state assignments using partitions, machine decomposition, state identification and fault detection experiments for sequential machines.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design** of switching circuits by threshold elements	-	4,5	1
CO-2	**Explain, analyze** and **design** of different fault detection and fault location experiments for combinational logic circuits and sequential machines.	4,5	3	-
CO-3	**Analyze** different techniques of failure tolerant design	-	3,4	-

CO-4	**Analysis and application** of algorithms for simplification of completely and incompletely specified sequential machines.	-	5	2,6
CO-5	**Choose** and **adapt techniques** to decompose the sequential machine into series components, parallel components and to achieve input independency, reduction in the output dependency	4,5	-	2,6
CO-6	**Design** and **Implement** homing experiments, distinguishing experiments and machine identification experiments.	-	-	4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2	2	2.2	2.5	1

Pre-requisites: Boolean Algebra, Logic Design

Contents:

1) **Threshold Logic:** Introductory Concepts, Synthesis of Threshold Networks. **07 Hrs**
2) **Reliable Design and Fault Diagnosis Hazards:** Hazards, Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure Tolerant Design, Quadded Logic. **08 Hrs**
3) **Capabilities, Minimization and Transformation of Sequential Machines:** The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite - State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. **08 Hrs**
4) **Structure of Sequential Machines:** Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines. **08 Hrs**
5) **State-Identifications and Fault-Detection Experiments:** Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences. **08 Hrs**

Reference Books:

1) Zvi Kohavi, "Switching and Finite Automata Theory", 2nd Edition. Tata McGraw Hill Edition, 2016.

2) Charles Roth Jr., "Digital Circuits and logic Design", Thomas Asia Pvt Ltd., Singapore, 6th Edition, 2004.

3) Parag K Lala, "Fault Tolerant And Fault Testable Hardware Design", Prentice Hall Inc. 1985.

4) Mishra & Chandrasekaran, "Theory of computer science Automata, Languages and Computation", 2nd Edition, PHI, 2004.

24PDEC103	Digital VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on understanding the construction details and electrical characteristics of MOSFETs, designing different digital applications of MOSFETs for the high speed and low power considerations.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction and the characteristics of MOS structures.	-	-	5
CO-2	**Design** of an Inverter with different loads.	-	4,5	-
CO-3	**Design** digital circuits using various design styles.	4,5	-	6
CO-4	**Discuss** Bi-CMOS gates and **Compare** the performance of CMOS and Bi-CMOS logic circuits.	4,5	6	-
CO-5	**Explore** various memory structures and low power design techniques.	-	4,5	-
CO-6	**Design** and Validate performance of digital systems.	4,5	1,3,6	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	1	2	2.6	2.6	1.6

Pre-requisites: Digital Circuit Design, Basic VLSI Design

Contents:

1) **MOS Field Effect Transistors (MOSFETs):** Device structure and physical operation, Current voltage characteristics, MOSFET circuits as DC, MOSFET as an amplifier and switch, Biasing in MOS Amplifier circuits. **08 Hrs**
2) **MOS Inverters:** Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter. MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints. **06 Hrs**
3) **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **06 Hrs**
4) **Semiconductor Memories**: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Non-volatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). **06 Hrs**
5) **Low-Power CMOS Logic Circuits:** Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits. **06 Hrs**
6) **Bi-CMOS Logic Circuits:** Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behaviour of BJTs, Basic Bi-CMOS Circuits: Static Behaviour, Switching Delay in Bi-CMOS Logic Circuits, Bi-CMOS Applications. **07 Hrs**

Activity beyond syllabus: Design of Digital Circuits using Cadence Software.

Reference Books:

1) Sung Mo Kang &Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition, 2003.
2) Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd., 2000.
3) Jan M. Rabaey, Massoud Pedram, “Low Power Design Methodologies” Kluwer Academic, 2010.
4) ADEL Sedra, Kenneth C Smith, "Microelectronic Circuits Theory & Applications," Oxford Publication, 2013.

24PDEC104	Nano Electronics	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the study of various nanostructures, their properties and applications. The course also focuses on understanding the physical, chemical and fabrication aspects of nanostructures and nanodevices at nanoscale, relevant to the field of electronics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Realize** the significance of Nanoelectronics, as an emerging area in the field of electronics.	3	-	-
CO-2	**Identify** various nanostructures, discuss their properties and applications	-	4	-
CO-3	**Analyze** and **discuss** the physical effects occurring in various nanodevices.	4	-	5
CO-4	**Classify** different microscopic techniques required to study novel properties of nanostructures occurring at nanoscale.	-	4	-
CO-5	**Compare** and **differentiate** various quantum structures, self-assembly techniques.	-	-	1
CO-6	**Discuss** the applications of nanostructures, in relevance to the field of electronics.	3	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	3	2.3	1	1

Pre-requisites:

Physics, Electronics, Engineering Mathematics, Material Science

Contents:

1) **Introduction:** Overview of nanoscience and engineering, Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale. Fabrication methods: Top down processes, Bottom up processes, methods describing the growth of nanomaterials, ordering of nanosystems. **08 Hrs**
2) **Characterization:** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques. **07 Hrs**
3) **Inorganic semiconductor nanostructures:** Overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.
   Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **08 Hrs**
4) **Fabrication techniques:** Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching. Strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.
   Physical processes: Modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural. **08 Hrs**
5) **Nanosensors:** Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future.
   Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures. **08 Hrs**

Reference Books:

1) Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.

2) Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology" , John Wiley, Copyright 2006, Reprint 2011.

3) T Pradeep, "Nano: The Essentials: Understanding Nanoscience and Nanotechnology", TMH, 2007.

4) Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, " Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

24PRMC105 Research Methodology and IPR (2-0-0) 2

Contact Hours: 26

Course Learning Objectives (CLOs): The students are expected to learn about the need and types of research, problem formulation, literature review, measurement, scaling, data collection, testing of hypothesis, result interpretation and report writing. Further, the students shall know about the intellectual property rights, copy rights, trademarks, patents, patents filing procedure, infringement & remedies and information technology act etc.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Formulate** the research problem, carryout literature survey and decide the methodology.	-	1	-
CO-2	**Use** measurement and scaling and **carryout** data collection.	-	1	-
CO-3	**Test** the hypothesis, **interpret** & **analyze** the results and **write** the report.	2	3	-
CO-4	**Explain** the need of IPR, copy right, patents, trademarks & the filing procedure and know about infringement, remedies and regulatory framework.	-	2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2.5	2	-	-	-

Pre-requisites: Branch specific course on problem analysis (Preferred)

Contents:

1) **Research Methodology:** Introduction, meaning of research, objectives of research, motivation in research, types of research, research approaches, research process, criteria of good research and problems encountered by researchers in India.

   Defining the Research Problem: Research problem, selecting the problem, technique involved in defining a problem, an illustration. **4 Hrs**

2) **Reviewing the literature:** How to review the literature, searching the existing literature, reviewing the selected literature.

   Research Design: Meaning of research design, need for research design, features of a good design, important concepts relating to research design, different research designs. **4 Hrs**

3) **Measurement and Scaling:** Measurement in research, measurement scales, sources of error in measurement.

   Data Collection: Collection of primary data, collection of secondary data. **4 Hrs**

4) **Testing of Hypotheses:** What is a Hypothesis? Basic concepts concerning testing of hypotheses, procedure for hypothesis testing, flow diagram for hypothesis testing, measuring the power of a hypothesis test, tests of hypotheses. **4 Hrs**

5) **Interpretation and Report Writing:** Meaning of interpretation, technique of interpretation, precaution in interpretation, significance of report writing, different steps in writing report, layout of the research report, precautions for writing research reports, plagiarism and its significance. **3 Hrs**

6) **Introduction to Intellectual Property Rights:** Meaning and conception of IPR, competing, rationale for protection, international conventions, world court.

   Copy right: Meaning, content, substance, ownership, primary, special rights, obligations, period, assignment, and relinquishment of copy rights. License and application for registration of copy right.

   Patents: Meaning of Patent, purpose and policy object of patent law, gains to inventor, application of patents, joint application, discovery and invention, patentable and non-patentable inventions.

   Industrial design: Concepts & Significance

   Trademarks: Definitions and conceptions of Trademark, advantages of registration, marks which are not registrable, known, and well-known trademarks, application for registration and procedure for registration, procedure, and certification of Trademarks.

   Infringement and Remedies: Meaning of infringement, acts of infringement.

   7 Hrs

Self Study:

The Information Technology Act: Definitions, certifying authority, meaning of compromise of digital signature, offences and penalties, applicability of IPRs, cybercrimes, adjudicating officer, violation, damages and penalties, Cyber regulation appellate tribunal, World Wide Web and domain names and cyber flying, Self study.

Reference Books:

1) C.R. Kothari, Gaurav Garg, Research Methodology: Methods and Techniques, New Age International, 4th Edition, 2018.

2) Ranjit Kumar, Research Methodology a step-by-step guide for beginners, SAGE Publications, 3rd Edition, 2011.

3) Fink A, Conducting Research Literature Reviews: From the Internet to Paper, Sage Publications, 2009.

4) N. K. Acharya, Text book on Intellectual Property Rights,4th Edition, Asia Law House, 2024.

24PDEL101 Digital Circuits Simulation Laboratory (0-0-2)1

Contact Hours:24

Course Learning Objectives (CLOs):

The course focuses on design of digital circuits and verifying the same by using Verilog code. The experiments are meant to give a good understanding of tools for realization of digital systems.

Course Outcomes (COs):

Description of the course outcomes: At the end of the course the students will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Demonstrate** logic gate **implementation** using Verilog code.	3		2,6
CO-2	**Design** different digital circuits and **verify** the functional simulation.	1,3	4,5	2,6
CO-3	**Design** a digital system for addition and multiplication operations.	1,3	4,5	2,6
CO-4	**Implement** sequential digital circuits on FPGA board.	1,3	4,5	2,6
CO-5	**Develop** LIFO and FIFO systems.	1,3	4	2,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3	1	3	2	2	1

Prerequisites: Digital Electronics, Verilog HDL

Contents:

Write Verilog codes to implement Digital circuits on FPGA/CPLD boards and performance testing may be done using pattern generator, Chip scope pro apart from verification by simulation with any of the frontend tools.

1) Write a Verilog code for 8:1 multiplexor in behavioral model, data flow and structural model.
2) Write a Verilog code for D and J-K FF using blocking and non- blocking statements.
3) Write a Verilog code for one bit full adder / subtractor.
4) Write Verilog code for the design of 8-bit.
   i. Carry Ripple Adder
   ii. Carry Look Ahead adder
   iii. Carry Skip Adder
5) Write Verilog Code for 8-bit.
   i. Array Multiplication
   ii. Booth Multiplication (Radix-4)
6) SWrite Verilog code for 4/8 bit
   i. Magnitude Comparator
   ii. LFSR
7) Write Verilog Code for 3-bit arbitrary counter to generate 0,1,2,3,6,5,7 and repeats.
8) Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg11101 (with and without overlap) any sequence can be specified.
9) Design a FIFO and LIFO buffers in Verilog and Verify its operation.
10) Write Verilog code to implement 8-bit ALU with arithmetic and logical operations.

Reference books:

1) Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using Verilog”, Elsevier, 2010.

2) Charles H. Roth, “Fundamentals of logic design”, Thomson Learning, 2004.

3) NC Launch User Guide Product Version 3.1 June 2000.

4) NC Verilog Simulator Help Product Version 3.1 June 2000.

II semester

24PDEC200	VLSI for Signal Processing	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The subject focuses on several high-level architectural transformations that can be used to design families of architectures for a given algorithm and develop knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** high-level architectural transformation for effective integrated circuit implementations	4	3	6
CO-2	**Analyze** high-level algorithmic transformation for effective integrated circuit implementations	4	3	6
CO-3	**Explain and apply** arithmetic strength reduction techniques	5	3	-
CO-4	**Explain and apply** numerical strength reduction techniques	5	3	-
CO-5	**Compare** the techniques of reducing the computational complexity	4	-	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	3	3	1

Pre-requisites: Digital Signal Processing, VLSI design

Contents:

1) **Introduction to Parallel Processing:** Parallelism in uniprocessor systems, Parallel Computer structures, architectural classification schemes, Parallel Processing Applications. Principles of Pipelining and Array Processors, an overlapped parallelism, instruction and arithmetic pipelines, data buffering and busing structures, SIMD array processors, parallel algorithm for array Processors. **08 Hrs**

2) **Iteration Bound, Pipelining, Parallel Processing, Retiming**: Introduction, Data-Flow graph representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power, Retiming Definitions and properties, solving systems of inequalities, Retiming Techniques. **09 Hrs**
3) **Unfolding and Folding**: Introduction, An algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, Applications of unfolding, folding transformation, register minimization techniques, register minimization in folded architectures, folding of multi-rate systems. **08 Hrs**
4) **Algorithmic Strength Reduction in filters and Transforms:** Introduction, Parallel FIR filters, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for Rank-Order filters. **09 Hrs**
5) **Pipelined and Parallel Recursive filters**: Introduction, pipeline interleaving in digital filters, pipelining in 1^{st}order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low-power IIR Filter Design using pipelining and parallel processing. **09 Hrs**
6) **Redundant Arithmetic and Numerical Strength Reduction:** Introduction, Redundant number representations, carry-free radix-2 addition and subtraction, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architectures, data format conversion, sub-expression elimination, multiple constant multiplication, sub-expression sharing in digital filters, additive and multiplicative number splitting. **09 Hrs**

Reference Books:

1) Kai Hwang & Faye A. Briggs, “Computer Architecture and Parallel Processing” McGraw-Hill Series, 1984.
2) Parhi, K.K., “VLSI Digital Signal Processing Systems: Design and Implementation”, John Wiley, 2007.
3) Wanhammar, L., “DSP Integrated Circuits”, Academic Press, 1999.
4) Magdy A. Bayoumi, “VLSI Design Methodologies for Architectures”, Kluwer Academic Publishers, 1994.
5) Mitra, S.K., “Digital Signal Processing: A Computer Based Approach”, McGraw Hill, 2007, 3rd edition.

24PDEC201	Advanced Embedded Systems	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the understanding of embedded processors, peripherals, bus standards, programming, tool chains and RTOS, through which targets design and development of embedded application.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the needs of Embedded systems. **Establish and correlate** the relevance of ARM Cortex M processor in context of Embedded Systems.	2	1	6
CO-2	**Develop** an insight into embedded system processor architecture and ISA. **Apply** the same for application development.	2,4	3,5	-
CO-3	**Understand** memory interfacing **and** interrupts/ exceptions. **Apply** the same for application development.	5	3,4	-
CO-4	**Evaluate and develop** applications for embedded systems by understanding the peripheral devices and bus standards.	5	3,4	1
CO-5	**Establish** the relevance of task management and RTOS in embedded systems.	5	3,4	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.3	3	2	2.25	2.7	1

Pre-requisites: Processor, controller and operating systems

Contents:

1) **ARM Cortex M processors:** Background and history, Advantages of the Cortex-M processors, General information about the Cortex-M3 processor, Features of the Cortex-M3 processor. **08 Hrs**
2) **Cortex-M3 Architecture:** Introduction to the architecture, Programmer's model, Behavior of the application program status register (APSR), Memory system, Exceptions and interrupts, System control block (SCB), Debug, Reset and reset sequence. **09 Hrs**
3) **Cortex-M3 Instruction Set:** Background to the instruction set in ARM Cortex-M, processors, Comparison of the instruction set in ARM Cortex-M processors, Understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly language (UAL), Instruction set, Barrel shifter, Accessing special instructions and special registers in programming **12 Hrs**
4) **Memory System:** Overview of memory system features, Memory map, Connecting the processor to memory and peripherals, Memory requirements, Memory endianness, Data alignment and unaligned data access support, Bit-band operations, Default memory access permissions, Memory access attributes, Exclusive accesses, Memory barriers, Memory system in a microcontroller. **12 Hrs**
5) **Exceptions and Interrupts:** Overview of exceptions and interrupts, Exception types, Overview of interrupt management, Definitions of priority, Vector table and vector table relocation, Interrupt inputs and pending behaviors, Exception sequence overview, Details of NVIC registers for interrupt control, Details of SCB registers for exception and interrupt control, Details of special registers for exception or interrupt masking, Example procedures in setting up interrupts, Software interrupts. **11 Hrs**

Reference Books:

1) Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Third edition, Newnes is an imprint of Elsevier, 2014
2) James K. Peckol, "Embedded Systems A Contemporary Design Tool", Second Edition, Wiley & Sons Ltd, 2019.
3) Wayne Wolf, "Computers as Components Principles of Embedded Computing System Design", Second edition, Morgan Kaufmann Publishers is an imprint of Elsevier, 2008.

24PDEL201 Advanced Embedded Systems Laboratory (0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The course focuses on the design and implementation of different applications of embedded systems using NXP LPC1768.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design** and **analyze** an application using C and ALPto **demonstrate** interworking between them	-	1,3	4,5
CO-2	**Demonstrate** interfacing of different peripherals to the microcontroller by **understanding** the aspects of electrical and delay parameters.	3,5	4	6
CO-3	**Exhibit** working of Interrupts and exceptions by proper **design** of ISR and stack policy.	-	1,4	1,3
CO-4	By usage of an **RTOS demonstrate** impact of scheduling policies with respect to completion time.	-	4,5	1,6
CO-5	**Demonstrate** IPC **and** data sharing in RTOS**.**	3	4,5	1,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.4	-	2.25	1.8	2	1

Pre-requisites:

Basics C and Assembly Programming along with controller architecture.

Contents:

1) Write an Assembly language program to calculate the sum and display the result for the additionof firstten numbers. SUM = 10+9+8+. +1
2) Write an Assembly language program to store data in RAM
3) Write a C program to output the “Hello World” message using UART
4) Write a C program to operate a buzzer using Cortex M3
5) Write a C program to display the temperature sensed using Cortex M3.

6) Write a C program to control stepper motor using Cortex M3.
7) To Test 4X4 keypad using Cortex M3 microcontrollers**.**
8) To test working of Interrupt using Cortex M3 microcontrollers.
9) To test on PWM technique using Cortex M3/M4 microcontrollers.
10) To locking a Mutex.

Reference Books:

1) Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Third edition, Newnes is an imprint of Elsevier, 2014.
2) James K. Peckol, Ph.D. ,"Embedded Systems A Contemporary Design Tool", Second Edition, Wiley & Sons Ltd, 2019.
3) Wayne Wolf, "Computers as Components Principles of Embedded Computing System Design", Second edition, Morgan Kaufmann Publishers is an imprint of Elsevier, 2008.

Electives

24PDEE250	**Advanced Computer Architecture**	**(4-0-0) 4**

Contact Hours: 52

Course Learning Objectives (CLOs):

The course deals with the understanding quantitative principles guiding the computer system design. It focuses on enhancing the performance by addressing parallelism at different levels such as Instruction, thread, task, job. Evaluates memory hierarchy, speculations, ISA, ALU architectures, choice of I/O is major motivation.

Course Outcomes:

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	Understand parallel computing concepts, identify opportunities for parallelism, and grasp principles of scalable performance.	1	5	4
CO-2	Explain processor and memory hierarchy, analyze advanced technologies, and understand memory optimization.	1	3	-
CO-3	Describe bus, cache, and shared	4	2	-

	memory, and evaluate their impact on data access in parallel systems.			
CO-4	Analyze multiprocessor architecture, synchronization, and design scalable systems using latency hiding.	-	1,3	6
CO-5	Comprehend parallel programming model, optimize code for parallelization, and utilize parallel programming tools effectively.	6	1,2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
MappingLevel	2.4	2	1.3	2	2	2

Course Contents:

1) **Theory of Parallelism:** Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers, Program and Network Properties, Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws. **12 Hrs**
2) **Processors and Memory Hierarchy:** Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. **11 Hrs**
3) **Memory Organization:** Bus systems, Cache Memory Organizations, Shared-Memory Organizations, Sequential and Weak Consistency Models. **10 Hrs**
4) **Parallel and Scalable Architectures:** Multiprocessors and Multicomputers, Multiporcessor system Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers, Message-Passing Mechanisms. Scalable, Multithreaded and Dataflow Architectures: Latency Hiding Techniques, Principles of Multithreading, Fine-Grained Multicomputers, Scalable and Multithreded Architectures, Dataflow and Hybrid Architectures. **10Hrs**
5) **Software for Parallel Programming:** Parallel Programming Model, Parallel Languages and Compilers, Dependence Analysis of Data Arrays, Code Optimization and Scheduling Loop Parallelization and Pipeline. **09Hrs**

Reference Books:

1) Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", McGraw-Hill, 1993.

2) John L. Hennessy and David A. Patterson "Computer Architecture A Quantitative Approach",6th edition, Morgan Kaufmann, 2019.

3) William Stallings "Computer Organization and Architecture Designing for Performance", 11th edition, Pearson, 2022.

4) Hesham El-Rewini, Mostafa Abd-El-Barr, "Advanced Computer Architecture and Parallel Processing", Wiley, 2005.

24PDEE251 Low Power Circuits & Systems (4-0-0)4

Contact Hours:52

Course Learning Objectives (CLOs):

The course focuses on basics and advanced techniques in the low power design. Describe the various power reduction and the power estimation methods and also explain power dissipation at all layers of design hierarchy. Apply State-of-the art approaches to power estimation and reduction. Practice the low power techniques using current generation design style and process technology.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** the sources of power dissipation in CMOS circuits.	-	4	-
CO-2	**Perform** power analysis using simulation based and probabilistic approaches.	-	3	4
CO-3	**Use** optimization and trade-off techniques to reduce power dissipation of the digital circuits.	4	5	6
CO-4	**Apply** practical low power design techniques and their analysis at various levels of design abstraction in the latest design automation environments.	4	5	6
CO-5	**Build** power efficient systems using advanced techniques.	6	4,5	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	2.2	2	1.6

Pre-requisites: Digital VLSI Design

Contents:

1) **Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **07 Hrs**
2) **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.
   Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **11 Hrs**
3) **Circuit:** Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.
   Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **09 Hrs**
4) **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **04 Hrs**
5) **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation. **04 Hrs**
6) **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division**.** **04 Hrs**
7) **Low power memory design:** Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM. **04 Hrs**
8) **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. **Advanced Techniques:** Adiabatic computation, pass transistor logic synthesis, Asynchronous circuits. **09 Hrs**

Reference Books:

1) Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.

2) Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies" Kluwer Academic, 2010.
3) Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.
4) A. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
5) A. Bellamour and M. I. Elmasri, " Low power VLSI CMOS circuit design", Kluwer Academic,1995.

24PDEE252 Artificial Intelligence & Machine Learning (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on introduction to the fundamental concepts in artificial Intelligence & machine learning. Topics covered are linear modeling, Bayesian approach, classification, clustering with popular machine learning algorithms in each topic. The course also discusses various issues related to the application of artificial intelligence using machine learning techniques.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Recognize** the characteristics of artificial intelligence systems that make it useful to real-world problems	-	3,1	2
CO-2	**Analyze** the situations of applying variety of mathematical models and algorithms for machine learning.	3	1	-
CO-3	**Compare** and **justify** various mathematical models and algorithms used in machine learning.	4,1	3	2
CO-4	**Justify** the selection of various classification and regression supervised/unsupervised learning problems of machine learning.	-	3,1	-
CO-5	**Select** and **implement** machine	4	3,1	

	learning techniques that are suitable for the applications under consideration.			
CO-6	**Evaluate** the performance of various machine learning algorithms		3	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	2.0	2.5	3.0	-	-

Pre-requisites: Basics of probability and statistics, Linear algebra

Contents:

1) **Introduction to Artificial Intelligence:** History of Artificial Intelligence, Propositional logic: Basics of propositional logic, Resolution, artificial intelligence applications, First order logic: Basics of first order logic, Certain knowledge representation: Taxonomic knowledge, frames, Non-monotonic logic. **06 Hrs**
2) **Linear Modeling-A Least Squares Approach:** Linear Modeling, Making Predictions, Vector/Matrix Notation, Non-Linear Response from a Linear Model, Generalization and Over-Fitting, Regularized Least Squares. **10 Hrs**
3) **Linear Modeling-A Maximum Likelihood Approach:** Errors as Noise, Random Variables and Probability, Popular Discrete Distributions, Continuous Random Variables - Density Functions, Popular Continuous Density Functions, Likelihood, The Bias-Variance Trade-off. **10 Hrs**
4) **The Bayesian Approach to Machine Learning**: A Coin Game, The Exact Posterior, The Three Scenarios, Marginal Likelihoods, Hyper parameters, Graphical Models, A Bayesian Treatment of the Olympic100m Data, Marginal Likelihood for Polynomial Model Order Selection. **10 Hrs**
5) **Bayesian Inference:** Non-Conjugate Models, Binary Responses, A Point Estimate - The Map Solution, The Laplace Approximation, Sampling Techniques. **08 Hrs**
6) **Classification & Clustering:** The General Problem, Probabilistic Classifiers, Non-Probabilistic Classifiers, Assessing Classification Performance, Discriminative and Generative Classifiers. The General Problem, K-Means Clustering, Mixture Models. **08 Hrs**

Activity beyond Syllabus: Program development for the machine learning Algorithms in MATLAB/ Python.

Reference Books:

1) Simon Rogers, Mark Girolami, "A First Course in Machine Learning", second edition, CRC Press, 2017.
2) Richard E. Neopolitan & Xia Jiang, "Artificial Intelligence with an introduction to machine learning", second edition, CRC press 2018.
3) Ethem Alpaydin, "Introduction to Machine Learning", Prentice Hall of India, Third edition, 2014
4) Mohssen Mohammed, Muhammad Badruddin Khan, Eihab Bashier, Mohammed Bashier, "Machine Learning, Algorithms and Applications", CRC Press, 2017.

24PDEE253 Image and Video Processing (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on image sampling, quantization, various image enhancement techniques, color image processing, image compression and fundamental concepts in video processing. The course also discusses various applications of image processing.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to PO (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** image sampling, quantization and model of color vision.	-	-	2
CO-2	**Apply** suitable image enhancement and restoration techniques.	-	4, 3	2
CO-3	**Differentiate** various filtering techniques in image processing.	-	3	2,1
CO-4	**Choose** appropriate feature extraction technique in analyzing the given image.	3	4	1
CO-5	**Select** appropriate image reconstruction algorithms and video processing techniques.	3	2	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	1.25	2.5	2.0	-	-

Pre-requisites: Digital signal processing**,** Stochastic and random process.

Contents:

1) **Image Perception:** Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. **06 Hrs**
2) **Image Sampling and Quantization:** Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. **06 Hrs**
3) **Image Enhancement:** Point operations, Histogram modeling, Spatial operations, Transform operations, Multi-spectral image enhancement, False color and pseudo-color, Color Image enhancement. **08 Hrs**
4) **Image Filtering & Restoration:** Image observation models, Inverse & Wiener filtering, Fourier domain filters, Smoothing splines and interpolation, Least squares filters, Generalized inverse, SVD and iterative methods, Maximum entropy restoration, Bayesian methods. **08 Hrs**
5) **Image Analysis & Computer Vision:** Spatial feature extraction, Transform features, Edge detection, Boundary extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification techniques. **08 Hrs**
6) **Image Reconstructions from Projections:** Introduction, Radon transform, Back projection operator, Projection theorem, Inverse Radon transform, Convolution/ Filter back-projection algorithm. **08 Hrs**
7) **Video Processing:** Fundamental concepts in video – Types of video signals, Analog video, Digital video, Color models in video, Video compression techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. **08 Hrs**

Activity beyond Syllabus: Seminar, Simulation based project.

Reference Books:

1) Anil K. Jain, “Fundamentals of Digital Image Processing," Pear son Education (Asia) Pvt. Ltd., Prentice Hall of India, 2004.

2) Z. Li and M.S. Drew, "Fundamentals of Multimedia", Pearson Education (Asia) Pvt. Ltd., 2004.
3) R. C. Gonzalez and R. E. Woods, "Digital Image Processing", 2nd edition, Pearson Education (Asia) Pvt. Ltd, Prentice Hall of India, 2004.
4) M. Tekalp, "Digital Video Processing", Prentice Hall, USA, 1995.
5) K.P.Soman, "Digital Signal & Image Processing', 1st edition, Elsevier, 2012.

24PDEE255 Cryptography and Network Security (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on techniques of enciphering and deciphering messages to maintain privacy of confidential data. It also discusses algorithms for authentication and integrity.

Course Outcomes (COs):

Description of Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** and **Apply** different symmetric cryptographic techniques to encrypt and decrypt data.	-	4,5	1,3
CO-2	**Describe** basic mathematical concepts and pseudorandom number generators required for cryptography.	4	-	3
CO-3	**Apply** and **estimate** different asymmetric cryptographic algorithms.	5	1	6
CO-4	**Explain** authentication functions to authenticate and protect the encrypted data.	5	-	6
CO-5	**Analyze** key exchange algorithms.	-	1	3
CO-6	**Discuss** algorithms for digital signature schemes.	-	4,5	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.5	-	1	2.33	2.5	1

Pre-requisites: Communication networks and finite fields

Contents:

1) **Symmetric Block Ciphers**: Terminology, Traditional Block Cipher structure, Data encryption standard (DES), Double DES, 3DES, The AES Cipher.
   Number Theory: Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Discrete logarithms. **12 Hrs**

2) **Public-Key Cryptosystems**: Principles, The RSA algorithm, Diffie- Hellman Key Exchange, Elgamal cryptographic system, Elliptic Curve Arithmetic, Elliptic Curve Cryptography. **09 Hrs**

3) **Pseudo-Random-Sequence Generators and Stream Ciphers:** Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Additive generators, GIFFORD. **08 Hrs**

4) **One-Way Hash Functions:** Background, SNEFRU, N-Hash, MD5, Secure Hash Algorithm [SHA], Message Authentication Codes. **06 Hrs**

5) **Digital Signatures:** Digital signatures, Elgamal Digital Signature Scheme, Digital signature Algorithm, RSA digital signatures, Elliptic Curve DSA. **09 Hrs**

6) **Electronic Mail Security:** Preety Good Privacy, S/MIME, IP Security Overview. **08 Hrs**

Reference Books:

1) William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN:978-93-325-1877-3.
2) Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X, 1996.
3) Behrouz A. Forouzan, "Cryptography and Network Security", 2nd Edition, TMH, 2007.
4) Atul Kahate, "Cryptography and Network Security", 3rd Edition, TMH, 2013.

24PDEE256	5G Wireless Communication	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses deals with LTE to 5G evolution, 5G Standardization, 5G NR, 5G core architecture, 5G channel access methods, protocols, 5G deployment, options, challenges and applications.

Course Outcomes:

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Explain** and **Analyze** LTE and LTE Advanced system architecture, protocol stack, channel structure, and radio resource management techniques.	3,4	-	1,2,6
CO-2	**Apply knowledge** of LTE downlink and uplink transport channel processing, including channel coding, and modulation for efficient communication.	1,3,4	-	2,6
CO-3	**Describe** 5G spectrum, technology components, and advanced techniques like MIMO and CoMP, **analyzing** their applications in 5G use cases.	1,3,4	-	2,6
CO-4	**Explain** 5G radio access technologies, including multi-carrier waveforms, orthogonal and non-orthogonal multiple access schemes, **evaluating** their efficiency for next-generation communication systems.	1,3,4	-	2,6
CO-5	**Describe** 5G network architecture and physical layer procedure, and **analyzing** their role in achieving efficient communication.	1,3,4	5	2,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.6	1	3	3	2	1

Prerequisites: Wireless Communications, Computer Communication Networks.

Contents:

1) **Long Term Evolution (LTE):** Evolution of Cellular Technologies, LTE System Architecture, LTE Protocol Architecture, Radio Interface Protocols, Hierarchical Channel structure of LTE, logical channels, transport channels, physical channels, Channel mapping, OFDMA Radio Resources: Frame structure, Physical Resource Blocks. **LTE Advanced:** LTE Advanced Requirements, LTE Advanced Technological Components. **10 Hrs**
2) **LTE Downlink Transport Channel Processing:** Downlink Transport Channel Processing Overview: Channel Coding Processing, Modulation processing; Downlink shared channels, Downlink Control Channels, Broadcast channels, Multicast channels, Downlink Physical Signals, Uplink Transport Channel processing. **10 Hrs**
3) **5G Spectrum, Technology Components and Use cases:** Introduction to 5G, 5G Spectrum, 5G Technology Components, **MIMO:** Introduction, Single User MIMO, Multi User MIMO, Cooperative MIMO, Downlink MIMO, Uplink MIMO; **CoMP:** Introduction, Downlink CoMP, Uplink CoMP; 5G targets and use cases: Extreme mobile broadband, Massive machine-type communication, Ultra-reliable machine-type communication with examples. **10 Hrs**
4) **5G Architecture:** Introduction, 5G Architecture Options, 5G Network Architecture: Core Architecture, RAN Architecture, Interfaces and Protocols, Network Slicing, Interworking with LTE. **06 Hrs**
5) **5G Radio Access Technologies:** Multi-carrier waveforms, Principle of Orthogonality: OFDM based waveforms, SC-FDE, Multicarrier with Filtering: Filter Bank based Multi-Carrier, Universal filtered OFDM, Non-orthogonal schemes for efficient multiple access: Non-orthogonal multiple access (NOMA), Sparse code multiple access (SCMA), Interleave division multiple access (IDMA). **08 Hrs**
6) **5G Physical Layer:** Introduction, 5G Multiple Access Principle, Physical Channels and Signals, Basic Structures for 5G Frame Structure, Downlink User Data Transmission, Uplink User Data Transmission, Uplink Signaling Transmission, Downlink Signaling Transmission. **08 Hrs**

Reference Books

1) Arunabh Ghosh, Jun Zhang, Jeffrey G. Andrewa, Rias Muhammed, “Fundamentals of LTE”, Pearson India Educaion Services Pvt. Ltd., 2018
2) Afif osseiran, Jose F, Monserrat, Patrick Marsch, “5G Mobile and Wireless Communications Technology”, Cambridge University Press, 2016.

3) Harri Holma, Antti Toskala, Takehiro Nakamura, “5G Technology 3GPP NEW RADIO”, John Wiley & Sons First Edition, 2020

4) Erik Dahlman, Stefan Parkvall, Johan Skold “5G NR:The Next Generation Wireless Access Technology”, Academic Press, 1st Edition, 2018.

5) Jonathan Rodriguez, “Fundamentals 5G Mobile Networks”, John Wiley & Sons, 1st Edition, 2015.