Academic Program: UG

Academic Year 2023-24

Syllabus

VII & VIII Semester B.E.

Electronics & Communication Engineering

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

Accredited by NBA under Tier-1 2023-2026

Ph: **0836-2447465 Fax: 0836-2464638 Web:** www.sdmcet.ac.in

SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for VII & VIII semester of UG program in Electronics and Communication Engineering is recommended by Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2023-24 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College – Vision and Mission

VISION:

To develop competent professionals with human values

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department- Vision and Mission

Vision

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

Mission

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, effective teaching learning process and the best of laboratory facilities.

M2: To encourage innovation, research culture and team work among students.

M3: Interact and work closely with industries and research organizations to accomplish knowledge at par.

M4: To train the students for attaining leadership with ethical values in developing and applying technology for the betterment of society and sustaining the global environment.

Program Educational Objectives (PEOs)

The Graduates, after a few years of Graduation will be able to:

I. **Apply** the latest in-depth knowledge in the field of Electronics and Communication Engineering with Mathematical applications to address real life challenges.
II. **Exhibit** the confidence for independent working and / or spirit to work cohesively with group.
III. **Readily** be accepted by the Industry globally.
IV. **Develop** design skills, fault diagnosis skills, communication skills and create research orientation.
V. **Inculcate** professional, social ethics and to possess awareness regarding societal responsibility, moral and safety related issues

Programme Outcomes (POs):

Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to

comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

13. Design economically and technically sound analog and / or digital systems based on the principles of signal processing, VLSI and communication Engineering (PO-13)

14. Integrate hardware – software, and apply programming practices to realize the solutions in electronics domain. (PO-14)

SDM COLLEGE OF ENGINEERING AND TECHNOLOGY, DHARWAD
Department of Electronics and Communication Engineering
VII Semester
Scheme of Teaching and Examinations 2023 – 24

Course Code	Course Category	Course Title	Teaching		Examination				
			L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
					Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration In Hrs.
18UECC700	PC	Antenna & Wave Propagation	4 - 0 - 0	4	50	100	3	-	-
18UECC701	PC	Computer Communication Networks	4 - 0 - 0	4	50	100	3	-	-
18UECE7XX	PE	**Program Elective-IV**	3 - 0 - 0	3	50	100	3	-	-
18UECO7XX	OE	**Open Elective**	3 - 0 - 0	3	50	100	3	-	-
18UECL702	PC	CCN Laboratory	0 - 0 - 2	1	50	--	--	50	3
18UECL703	PC	Major Project Phase-1	0- 0 -4	2	50	--	--	50	3
18UECL704	PC	Internship	4 w e e k s	2	50	--	--	50	3
	Total		**14 - 0 -6**	**19**	**350**	**400**		**150**	

18UECE7XX	PE	**Program Elective-IV**
18UECE710		MEMS
18UECE711		ASIC Design
18UECE712		VLSI DSP Systems
18UECE713		Optical Fiber Communication
18UECO7XX	OE	**Open Elective (For All Branches)**
18UECO720		Machine Learning
18UECO721		Pattern Recognition
18UECO722		Multi Core Programming
18UECO723		Mobile Computing

PC- Program Core, PE-Program Elective, OE- Open Elective

SDM COLLEGE OF ENGINEERING AND TECHNOLOGY, DHARWAD
Department of Electronics and Communication Engineering
VIII Semester
Scheme of Teaching and Examinations 2023 – 24

Course Code	Course Category	Course Title	Teaching		Examination				
			L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
					Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration In Hrs.
18UECC800	PC	Wireless Communication	4 - 0 - 0	4	50	100	3	-	-
18UECE8XX	PE	**Program Elective-V**	3 - 0 - 0	3	50	100	3	-	-
18UECO8XX	OE	**Open Elective**	3 - 0 - 0	3	50	100	3	--	--
18UECL801	PC	Technical Seminar	0 - 0 - 2	1	50	--	--	--	--
18UECL802	PC	Major Project Phase-2	0-0 -12	7	50	--	--	50	3
	Total		**10- 0 - 14**	**18**	**250**	**300**	**--**	**50**	**--**

18UECE8XX	PE	**Program Elective-V**
18UECE810		Adhoc Wireless Networks
18UECE811		Re-configurable Design
18UECE812		Low Power VLSI Design
18UECE813		Digital Signal Compression
18UECO8XX	OE	**Open Elective (For All Branches)**
18UECO820		DSP Architecture
18UECO821		CAD for VLSI
18UECO822		Operation Research
18UECO823		Advanced Computer Architecture

PC- Program Core, PE-Program Elective and OE- Open Elective

VII Semester

18UECC700	Antennas & Wave Propagation	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs): The course focuses on the theory and applications of various types of Antennas. Various methods of analysis of antennas are discussed. The properties and characteristics of various types of Antennas are discussed. The course ends with a discussion of various aspects of Radio Wave Propagation.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Discuss** the basics of Antennas.	-	12	1
CO-2	**Analyze** point sources, arrays of point sources and their characteristics.	-	2	-
CO-3	**Derive** field equations for short dipole, small loop and other types of antennas.	4	1,2	-
CO-4	**Discuss** the structures, properties and characteristics of various types of antennas.	1	4	13,5
CO-5	**Discuss** various modes of radio wave propagation.	1	12	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.25	2.0	-	3.0	1.0	-	-	-	-	-	-	2.0	2.0	-

Pre-requisites: Electromagnetic Theory

Contents:

Unit-I

Antenna Basics: Introduction, Basic Antenna parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Directivity & Resolution, Antenna apertures, Effective height, Radio Communication link, Fields from oscillating dipole, Antenna Field Zones, Linear, Elliptical & Circular polarization.

09 Hrs

Unit-II

Point Sources And Their Arrays: Introduction, Point Source defined, Power patterns, Power theorem, Radiation intensity, Examples of Power patterns, Field patterns, Phase patterns, Arrays of two Isotropic Point sources, Non-Isotropic but similar Point Sources and Principle of pattern multiplication, Non-isotropic and Dissimilar Point sources, Linear Arrays of n Isotropic Point sources of equal amplitude and spacing. **09 Hrs**

Unit-III

Electric Dipoles And Thin Linear Antennas: Introduction, Short electric dipole, Fields of a short dipole, Radiation resistance of short dipole, Radiation resistance of lambda/2 antenna, Thin linear antenna, Micro strip arrays, Low side lobe arrays, Long wire antenna, Folded dipole antennas.

Loop, Slot, Patch And Horn Antenna: Introduction, Small loop, Comparison of far fields of small loop and short dipole, Loop antenna general case, Far field patterns of Circular Loop, Radiation resistance of loops, Directivity, Slot antennas, Babinet's Principle and Complementary antennas, Impedance of Complementary and Slot antennas, Patch antennas, Horn antennas, Rectangular horn antennas. **12Hrs**

Unit-IV

Antenna Types: Helical antenna, Yagi-Uda array, Corner reflectors, Parabolic reflectors, Log Periodic antenna, Lens antenna, Antennas for special applications – Sleeve antenna, Turnstile antenna, Omni directional antennas, Antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna. **11Hrs**

Unit-V

Radio Wave Propagation: Introduction, Ground wave propagation, Free Space propagation, Ground reflection, Surface wave, Diffraction. Tropospheric propagation: Tropospheric scatter, Ionospheric propagation, Structure of the Ionosphere, Electrical properties of the Ionosphere, Effects of earth's magnetic field, Propagation characteristics of Radio waves for different frequencies, Simple definitions. **11Hrs**

Reference Books:

1. John D. Kraus, Ronald J. Marhefka, Ahmad S. Khan "Antennas for all Applications", 4/e, McGraw-Hill edition, 2010.

2. Harish and Sachidananda, “Antennas and Wave Propagation”, Oxford Press, 2007.
3. C. A.Balanis, “Antenna Theory Analysis and Design”, 3/e,John Wiley India Pvt. Ltd., 2008.,John Wiley, 2003.
4. G. S. N. Raju, “Antennas and Wave Propagation”, Pearson Education, 2005
5. K. D. Prasad “Antenna & Wave Propagation”, Satya Prakashana, New Delhi, 1999.
6. D. Kumaraswamy, M. S. Srinivas, K. Giridhar, “Antennas & Propagation”, Pooja Publications, Bangalore, 2009-10.

18UECC701 Computer Communication Networks (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the process of data communication in computer network through the layered architecture. It also deals with the IEEE standards and various protocols at different layers.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Exploring** layered architecture in OSI and TCP/IP network models and **Explain** the functionalities of layers.	-	1	-
CO-2	**Analyze** and **compare** various protocols for framing, error and flow control and medium access.	1,2	3,14	-
CO-3	**Identify** the IEEE standards for wired and wireless networking and **discuss** the significance of connecting devices in networking.	-	1,3	2
CO-4	**Understand** IPv4 and IPv6 addressing in internetworking and **identify** the need for transition from IPv4 to IPv6	2,3	1	-
CO-5	**Analyze and compare** different routing protocols in network layer and protocols for process to process delivery of information in transport layer.	-	2,3	4

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.25	2.25	2.25	1.0		-	-	-	-	-	-	-	-	2

Pre-requisites: Basics of communication.

Contents:

Unit-I

Introduction to computer networks: Data Communication, Networks, The Internet, Protocols and Standards.

Network Models: Layered tasks, OSI Model, Layers in OSI model, TCP/IP Protocol Suite, Addressing levels

Using Telephone and cable networks for data transmission: Telephone networks, Dial up modem, DSL, Cable TV for data transmission.

10Hrs

Unit-II

Data Link Control: Framing, Flow and error control, Noiseless channels and noisy channels, Protocols Piggybacking

Multiple Access protocol: Random access, Controlled access, Channelization.

11 Hrs

Unit-III

Wired LANs - Ethernet: IEEE standards, Standard Ethernet, Changes in the Standards.

Wireless LANs: IEEE 802.11, Bluetooth.

Connecting LANs, Backbone Networks and Virtual LANs: Connecting devices, Back bone Networks, Virtual LANs **10 Hrs**

Unit-IV

Network Layer: Logical addressing Ipv4 addresses, classful and classless addressing, network address translations (NAT),Ipv6 addresses, Internetworking, Ipv4, Ipv6, Transition from Ipv4 to Ipv6. **10 Hrs**

Unit-V

Network Layer - Delivery, Forwarding and Routing: Delivery, Forwarding techniques, Unicast Routing Protocols, distance vector routing, link state routing.

Transport layer-Process to process Delivery, User Datagram Protocol (UDP), Transmission Control Protocol (TCP). **11Hrs**

Reference Books:

1) B. Forouzan, **"Data Communication and Networking"**, 4th Edition, TMH, 2006.
2) James F. Kurose, Keith W. Ross "**Computer Networks"**, Pearson Education, 2nd Edition, 2003.
3) Wayne Tomasi, **"Introduction to Data communication and Networking"**, Pearson Education, 2007.
4) Andrew S. Tanenbaum, "**Computer Networks**", 4th Edition, Pearson Education, 2009.

18UECE710	MEMS	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the study of various micro-electromechanical systems. The course discusses different fabrication techniques, modeling aspects and transduction principles of various electromechanical sensors, actuators at micro and nanoscale.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Appreciate** the significance of MEMS, as an emerging area in the field of electronics.	1	-	2
CO-2	**Identify** various micro sensors and actuators used for electromechanical applications.	2	-	4
CO-3	**Discuss** the processes involved in the fabrication of different micro sensors and micro actuators.	-	2	5

CO-4	**Design** simple micro sensors and actuators using CAD Tools and **perform** simulation.	5	2,3	13
CO-5	**Classify** various micro system packaging technologies related to MEMS.	2	3	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	2	2	1	2	-	-	-	-	-	-	-	1	-

Pre-requisites: Physics, Electronics, Material Science, Basic Mechanical principles

Contents:

Unit-I

Overview of MEMS & Microsystems: MEMS & Microsystems, typical MEMS and micro system products — features of MEMS, multidisciplinary nature of microsystems design and manufacture, applications of microsystems.

Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling in electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer. **8 Hrs**

Unit-II

Transduction Principles in MEMS & Microsystems: Introduction, micro sensors, electromechanical transducers, micro actuation principles, MEMS with micro actuators, Micro accelerometers, MEMS switches, micro relays, MEMS inductors and capacitors. **8 Hrs**

Unit-III

Microsystems Fabrication Process: Introduction, photolithography, ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, MEMS fabrication processes: Surface micro-machining, Bulk micromachining, LIGA process. **8 Hrs**

Unit-IV

Micro System Design and Modeling: Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: Multiphysics/ Intellisuite/MEMS CAD, Features and Design considerations of RF MEMS, Design

considerations of Optical MEMS, Design and Modeling: Case studies- i) Cantilever beam ii) Micro switches **8 Hrs**

Unit-V

Micro system packaging: Over view of mechanical packaging of micro electronics micro system packaging, interfaces in micro system packaging, packaging technologies in MEMS. **7 Hrs**

Reference Books:

1) K. Tai Ran Hsu, "MEMS and Micro Systems: Design and Manufacture", Tata McGraw Hill, 2002.
2) Boca Raton, "MEMS and NEMS: Systems, Devices and Structures", CRC Press, 2002.
3) J. W. Gardner and V. K. Varadan, "Micro Sensors MEMS and SMART Devices", John Wiley, 2002 N. Maluf, "Introduction to Micro Mechanical Systems Engineering, Artech House", Norwood, MA, 2000.
4) V.K.Varadan, K.J.Vinoy and K.A.Jose, "RF MEMS and their Applications", Wiley India Pvt Ltd, Reprint 2011.

18UECE711	**ASIC Design**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on ASIC design flow, challenges in the design, verification phase, and various circuit examples and widely used ASIC tools.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Interpret** the types of ASIC design flow and its concepts.	-	1	-
CO-2	**Analyze** the challenges in designing complicated digital circuits and its CMOS Implementations.	-	1,2	3
CO-3	**Apply** the Partitioning & Floor-planning Techniques	3	4	-

CO-4	**Evaluate** placement and routing techniques for ASIC.	5	-	1,2
CO-5	**Design** of SOC based Architectures and its applications.	13,14	12	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.66	1.5	2	2	3	-	-	-	-	-	-	2	3	3

Pre-requisites: FPGA and microcontroller architecture.

Contents:

Unit-I

Introduction To ASICs: Types of ASICs, Full-Custom ASICs, Standard cell based ASICs, Gate array based ASICs, Channelled gate array, channel-less gate array, structured gate array, Programmable logic devices (PLD), Field–programmable gate arrays (FPGA),ASIC Design flow, Economics of ASICs with Example. **6 Hrs**

Unit-II

Logic Design: CMOS Implementations, Transistor Sizing, Logical Effort: Predicting delays, logical areas and logical efficiency, logical paths, Multi stage cells, Optimum delay, Optimum number of stages, RTL design, Concept of RTL Linting, Clock domain Crossing. **8 Hrs**

Unit-III

Partitioning & Floor-planning: Partitioning Methods, Measuring Connectivity, Constructive and Iterative Partitioning, The Kernighan–Lin Algorithm, The Ratio-Cut Algorithm**.** Floor-planning goals and objectives, floor planning tools, I/O and powerplanning, clock system planning. **8Hrs**

Unit-IV

Placement & Routing: placement goals and objectives, placement algorithms, iterative placement, Time Driven Placement Algorithm, Global routing and types, Detailed routing: Left edge Algorithm, Special routing**.** **8 Hrs**

Unit- V

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, On-Chip

Communication Architecture Standards, Low-Power SoC Design**.** **9 Hrs**

Activity beyond Syllabus: Seminar on Fabrication Techniques

Reference Books:

1) M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson Education,1/e 2002.
2) Jose E. France, YannisTsividis, “Design of Analog–Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 2/e 1993.
3) Malcolm R Haskard, Lan C, May, “Analog VLSI Design – NMOS and CMOS”, Prentice Hall, 1998.
4) Hoi-Jun Yoo, KangminLeeand JunKyong Kim, “Low-Power NoC for High-Performance SoC Design”, CRC Press, 2008

18UECE712	**VLSI DSP Systems**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

VLSI DSP Systems focuses on various concepts and architectural requirements of a digital signal processing system, with a view point of its implementation in VLSI.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** various parallel processing architectures	-	1, 2	-
CO-2	**Analyze and describe** various techniques of representations of DSP circuits and retiming.	-	3,5	-
CO-3	**Explain and apply** arithmetic strength reduction techniques.	-	3	12
CO-4	**Describe and apply** Pipelined and Parallel Recursive filters implementation.	-	3, 12, 13	-

CO-5	**Explain** Redundant Arithmetic and **apply** numerical strength reduction techniques.	-	3, 13	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2	2	2	-	2	-	-	-	-	-	-	1.3	2	-

Prerequisites: Digital Signal Processing

Contents:

Unit-I

Introduction to Parallel Processing: Parallelism in uniprocessor systems, Parallel Computer structures, architectural classification schemes, Parallel Processing Applications. Principles of Pipelining and Array Processors, an overlapped parallelism, instruction and arithmetic pipelines, data buffering and busing structures, SIMD array processors, parallel algorithm for array Processors. **08Hrs**

Unit-II

Iteration Bound, Pipelining, Parallel Processing, Retiming: Introduction, Data-Flow graph representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power, Retiming Definitions and properties, solving systems of inequalities, Retiming Techniques. **08Hrs**

Unit-III

Algorithmic Strength Reduction in filters and Transforms: Introduction, Parallel FIR filters, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for Rank-Order filters. **07Hrs**

Unit-IV

Pipelined and Parallel Recursive filters: Introduction, pipeline interleaving in digital filters, pipelining in 1^{st}order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low-power IIR Filter Design using pipelining and parallel processing. **08Hrs**

Unit-V

Redundant Arithmetic and Numerical Strength Reduction: Introduction, Redundant number representations, carry-free radix-2 addition and subtraction, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architectures, data format conversion, sub expression elimination, multiple constant multiplication, sub

expression sharing in digital filters, additive and multiplicative number splitting.

08 Hrs

Reference Books:

1) Computer Architecture and Parallel Processing by Kai Hwang & Faye A. Briggs, McGraw-Hill Series, 1984.
2) Parhi, K.K., "VLSI Digital Signal Processing Systems: Design and Implementation", John Wiley,2007.
3) Wanhammar, L., DSP Integrated Circuits, Academic Press, 1999.
4) Magdy A. Bayoumi, VLSI Design Methodologies for Architectures, Kluwer Academic Publishers, 1994.

18UECE713 Optical Fiber Communication (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on principles of Optical Fiber Communication, devices involved in communication system and challenges in Optical Fiber Communication networks.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Classify** the structures of Optical fiber and types and **Calculate** their different parameters in single mode and Multimode operation.	13	-	1
CO-2	**Illustrate** the optical fiber channel impairments and **analyze** various types of optical fiber coupling losses.	4,13	1,2	-
CO-3	**Discuss** different Optical sources and detector with their principles and **analyze** link power and rise time budget schemes for optical fiber links.	4,13	2,3	1
CO-4	**Describe** the working principles of WDM with different active and passive devices of optical fiber link.	3,13	1,2	-
CO-5	**Explain** concepts, working principles of	-	3,13	1,2,12

	different types of optical networks and their structures.			

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.5	1.75	2.33	1.5								1	2.8	

Pre-requisites: Optical physics, Analog Communication, Digital Communication

Contents:

Unit-I

Optical fiber Communications: Historical development, The general system, Advantages of optical fiber communication, Optical fiber wave guides: Ray theory transmission, Modes in planar guide, Phase and group velocity, And Cylindrical fiber: Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic cystalfibers (PCF)

09 Hrs

Unit-II

Transmission characteristics of optical fiber: Attenuation, Material absorption losses, Linear scattering losses, Nonlinear scattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber. Optical Fiber Connectors: Fiber alignment and joint loss, Fiber splices, Fiber connectors, Fiber couplers. **09 Hrs**

Unit-III

Optical sources: Energy Bands, Direct and Indirect Band gaps, Light Emitting diodes: LED Structures, Light Source Materials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant frequencies, Laser Diode structures and their principles.

Photo detectors: Physical principles of Photodiodes, Photo detector noise, Detector responsetime. **07 Hrs**

Unit-IV

Optical Receiver: Optical Receiver Operation: Error sources, Receiver sensitivity, Quantum Limit, Introduction, point–to–point links, System considerations, link power budget, rise-time budget calculations. Short wavelength band and transmission distance for single mode fibers, Power penalties, nodal noise and chirping.

Analog Links: Analog links — Introduction, overview of analog links, CNR, multichannel transmission techniques, key link parameters, Radio over fiber links, microwave photonics. **07 Hrs**

Unit-V

WDM Concepts and Components : Overview of WDM, Operational Principles of WDM, WDM standards, Multiplexers, Isolators and Circulators, Fiber grating filters,Dielectric Thin-Film Filters, Diffraction Gratings, Active Optical Components, Tunable light sources.

Optical Networks: Optical Networks concepts, Network Topologies, Introduction to SONET/SDH networks, Optical Add/Drop Multiplexing, Wavelength Division Multiplexing (WDM) Concepts. Revolution of optical networks in India. **07 Hrs**

Reference Books:

1) Gerd Keiser, "Optical Fiber Communication",5th Edition,McGraw Hill Education (India) Private Limited,2015.
2) John M Senior, "Optical Fiber Communications, Principles and Practice",3rd Edition, Pearson Education, 2010.
3) Rama Swamy & Sivarajan, "Optical Networks",2nd edition,Elsevier publishers, 2010.
4) Govind P .Agarwal,"Fiber Optic Communication Systems",3rd edition,John Wiley India.2001.

18UECO720	Machine Learning	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on introduction to the fundamental concepts in machine learning. Topics covered are linear models, generative models, classification, clustering with popular machine learning algorithms. The course also delves into selected topics of deep learning.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Recognize** the need and role of machine learning in engineering and artificial intelligence.	-	2,4	1

CO2	**Design** and implement machine learning solutions to classification and regression problems; and be able to evaluate and interpret the results of the algorithms.	-	2,3	1
CO-3	**Apply** the machine learning algorithms to the identified real-world problem, optimize the models learnt and evaluate models based on the expected accuracy.	12	2,4	1,5
CO-4	**Calculate** weight gradients in a feed forward neural network using back propagation algorithm.	-	2	1
CO-5	**Identify** the deep learning algorithms which are more appropriate for various types of learning tasks in various domains.	12	5	13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	2	2	2	1.5	-	-	-	-	-	-	3	1	-

Pre-requisites: Digital signal processing, Digital image processing, Stochastic and random process.

Contents:

Unit-I

Introduction: Basic definitions, Machine learning: what and why? Supervised learning, Unsupervised learning. Probability- A brief review of probability theory.

08Hrs

Unit-II

Linear Models for Regression: Linear Basis Function Models, Bayesian Linear Regression, The Evidence Approximation.

Linear Models for Classification: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Models, Bayesian Logistic Regression.

08Hrs

Unit-III

Generative models for discrete data: Introduction, Bayesian concept learning, The beta-binomial model, The Dirichlet-multinomial model, Naive Bayes classifiers.

08Hrs

Unit-IV

Neural Networks: Feed-forward Network Functions, Network Training, Error Backpropagation, The Hessian Matrix, Regularization in Neural Networks, Bayesian Neural Networks.

Kernel Methods: Dual Representations, Constructing Kernels, Gaussian Processes.

Sparse Kernel Machines: Maximum Margin Classifiers, Relevance Vector Machines. **07Hrs**

Unit-V

Deep learning: Introduction, Deep generative models, Deep neural networks, Applications of deep networks.

Convolutional Networks: The Convolution Operation, Motivation, Pooling, Variants of the Basic Convolution Function, Data, Efficient Convolution Algorithms. **08Hrs**

Reference Books:

1) Christopher Bishop, “Pattern Recognition and Machine Learning”, Springer, 2006

2) Kevin Murphy, “Machine Learning - a Probabilistic Perspective”, MIT Press, 2012.

3)Joachims, “Learning to Classify Text using Support Vector Machines”,Kluwer, 2002.

4) Ian Goodfellow and YoshuaBengio and Aaron Courville, “Deep Learning”, An MIT Press book.

18UECO721	Pattern Recognition	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on various pattern recognition techniques such as statistical and parametric decision making. Students will also be introduced to the concepts of artificial neural network.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** the principle of various pattern recognition techniques.			1

CO-2	**Distinguish** various pattern recognition techniques.		12	1
CO-3	**Apply** a pattern recognition technique to a given data.	2,3	13	5
CO-4	**Choose** between pattern recognition techniques to satisfy given requirement		2,3	12
CO-5	**Calculate** weight gradients in a feed forward neural network using back propagation algorithm.		2	1

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	2.33	3	-	1	-	-	-	-	-	-	1.5	2	-

Pre-requisites: Digital signal processing, Digital image processing, Stochastic and random process.

Contents:

Unit-I

Introduction: Applications of pattern recognition, statistical decision theory, image processing and analysis, probability of events, random variables, Joint distributions and densities, moments of random variables, estimation of parameters from samples, minimum risk estimators. **08 Hrs**

Unit-II

Statistical Decision Making: Introduction, Baye's Theorem, multiple features, conditionally independent features, decision boundaries, unequal costs of error, estimation of error rates, the leaving-one-out technique. Characteristic curves, estimating the composition of populations. **08Hrs**

Unit-III

Nonparametric Decision Making: Introduction, histograms, Kernel and window estimators, nearest neighbor classification techniques, adaptive decision boundaries, adaptive discriminate Functions, minimum squared error discriminate functions, choosing a decision making technique. **08Hrs**

Unit-IV

Clustering: Introduction, hierarchical clustering, partitioned clustering. **07 Hrs**

Unit-V

Artificial Neural Networks: Introduction, nets without hidden layers, Nets with hidden layers, the back propagation algorithms, Hopfield nets an application.**08 Hrs**

Reference Books:

1) Earl Gose, Richard Johnsonburg and Steve Joust, “Pattern Recognition and Image Analysis”, PHI, 2003
2) Robert J Schalkoff, “Pattern recognition: Statistical, Structural and neural approaches”, 1/e, John Wiley.
3) Christopher Bishop, “Pattern Recognition and Machine Learning”, Springer,2006.
4) Richard O. Duda, Peter E. Hart, David G. Stork, “ Pattern Recognition”, 2/e, Wiley, 2000.

18UECO722 Multicore Programming (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on basic concepts of Multi Core programming and various practical models of Multi Core programming. Aims to provide basic insight into multicore architecture along with Parallel Programming concepts. It also exposes OpenMP and MPI constructs, threading APIs and multicore software development and debugging techniques

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** different parallel computing architectures and their applicability.	1,2		4,10
CO-2	**Develop** an insight into multicore hardware architecture and threading and synchronization and **utilize** it to build applications.	1, 2,14	3	4
CO-3	**Illustrate** programming using OpenMP and MPI.	2,3,4,5	13,14	
CO-4	Examine the threading APIs.	1,3,5		14
CO-5	Distinguish multiprocessor software development products and debugging techniques.	5,12	4	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	3	2.7	1.8	3	-	-	-	-	-	-	3	2	2

Pre-requisites: Probability theory, Communication Systems

Contents:

UNIT-I

INTRODUCTION TO MULTI-CORE ARCHITECTURE: Motivation for Concurrency in Software, Parallel Computing Platforms (SIMD & MIMD systems, an overview of Single-Core, Multi-Processor, Multi-Core Architectures), Parallel Computing in Microprocessors, Differentiating Multi-Core Architectures from Hyper-Threading Technology, Multi-threading on Single-Core versus Multi-Core Platforms, Understanding Performance, Amdahl's Law, Gustafson's Law **08 Hrs.**

Unit-II

MULTI-CORE PROCESSORS: An Overview of Software Threading Defining Threads, System View of Threads: Threading above the Operating System, Threads inside the OS, Threads inside the Hardware, Application Programming Models and Threading, Virtual Environment: Virtual Machines and Platforms Runtime Virtualization, System Virtualization**.**

PARALLEL PROGRAMMING FUNDAMENTAL CONCEPTS: Designing for threads, parallel programming patterns, Threading and parallel programming constructs: Synchronization, Critical sections, Deadlock, Synchronization Primitives, and Messages **08 Hrs.**

Unit-III

OPENMP PROGRAMMING: OpenMP Challenges in Threading a loop, Minimizing Threading overhead, Performance oriented Programming, Library Functions. Solutions to parallel programming problems: Data races, deadlocks and Livelocks Non-blocking algorithms, Memory and cache related issues.

MPI PROGRAMMING: Message-Passing Model, Message-Passing Interface, MPI functions, Compiling and running MPI Programs, collective communication, data decomposition, Point-to-point communication – MPI Library. **08 Hrs.**

Unit-IV

THREADING API'S: Threading APIs for Microsoft Windows, Threading APIs for Microsoft .NET Framework: Creating Threads, Managing Threads, Thread Pools, Thread Synchronization, POSIX Threads: Creating Threads, Managing Threads, Thread Synchronization, Signaling, Compilation and Linking **07 Hrs.**

Unit-V

MULTI-THREADED DEBUGGING TECHNIQUES: General Debug Techniques, Debugging Multi-threaded Applications in Windows: Threads Window, Trace points, Breakpoint Filters, Naming Threads, Multi-threaded Debugging Using GDB.

MULTI-CORE PROCESSORS SOFTWARE DEVELOPMENT PRODUCTS: An Overview of Software tools on Multi-Core Processors, Intel Software Development Products: overview, Thread Checker, Compilers: OpenMP, Software-based Speculative Pre computation, Compiler Optimization and Cache Optimization, Debugger , Intel Libraries, Intel Threading Building Blocks , VTune Performance Analyzer , Thread Profiler , MPI Programming :Intel Support for MPI **08 Hrs.**

Reference Books:

1) ShameemAkhter and Jason Roberts, “Multi-core Programming- Increasing Performance through Software Multi-Threading”, 1st Edition, Intel Press, 2006.
2) Michael J Quinn, “Parallel programming in C with MPI and OpenMP”, 2nd Edition, Tata McGraw Hill, 2007.
3) Peter S. Pacheco, “An Introduction to Parallel Programming”,Morgan Kaufmann Publishers is an imprint of Elsevier,2011
4)

18UECO723	**Mobile Computing**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on basics of mobile communications, mobile computing, GSM systems, networking, transport and application layer protocols, different mobile platforms and application development and security issues.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Explain the basics of mobile telecommunication systems	-	-	1,4,6,7
CO-2	Illustrate the generations of telecommunication systems in wireless networks	-	1,2,4,5	12,13,14

CO-3	Determine the functionality of MAC, network layer and Identify a routing protocol for a given Adhoc network	-	2,4	12,13,14
CO-4	Explain the functionality of Transport and Application layers	-	1,2,4,10	-
CO-5	Develop a mobile application using android/blackberry/ios/Windows SDK	1,2,3,4,5,13, 14	-	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.0	2.25	3.0	2.0	2.5	1.0	1.0	-	-	2.0	-	1.0	1.33	1.33

Pre-requisites: Wireless communication, Digital communication Computer Communication Networks;

Contents:

Unit-I

Introduction: Mobile Communications, Mobile Computing– Paradigm, Promises/Novel Applications and Impediments and Architecture; Mobile and Hand held Devices, Limitations of Mobile and Handheld Devices.

GSM–Services, System Architecture, Radio Interfaces, Protocols, Localization, Calling, Handover, Security, New Data Services, GPRS,CSHSD, DECT. **08 Hrs**

Unit-II

(Wireless) Medium Access Control (MAC): Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA, Wireless LAN / (IEEE802.11)

Mobile Network Layer: IP and Mobile IP Network Layers, Packet Delivery and Handover Management, Location Management, Registration, Tunnelling and Encapsulation, Route Optimization, DHCP. **08 Hrs**

Unit-III

Mobile Transport Layer: Conventional TCP/IP Protocols, Indirect TCP, Snooping TCP, Mobile TCP, Other Transport Layer Protocols for Mobile Networks.

Database Issues: Data base Hoarding & Caching Techniques, Client-Server Computing & Adaptation, Transactional Models, Query processing, Data Recovery Process & QoS Issues. **07 Hrs**

Unit-IV

Data Dissemination and Synchronization: Communications Asymmetry, Classification of Data Delivery Mechanisms, Data Dissemination, Broadcast Models, Selective Tuning and Indexing Methods ,Data Synchronization–Introduction, Software, and Protocols. **09 Hrs**

Unit-V

Mobile Device Operating Systems – Special Constraints & Requirements – Commercial Mobile Operating Systems – Software Development Kit: iOS, Android, BlackBerry, Windows Phone–M Commerce–Structure–Pros & Cons–Mobile Payment System–Security Issues.

Protocols and Platforms for Mobile Computing: WAP,Bluetooth,XML,J2ME, Java Card, Palm OS, Windows CE, Symbian OS, Linux for Mobile Devices, Android. **07 Hrs**

Reference Books:

1) Jochen Schiller, “Mobile Communications” ,PHI,SecondEdition,2003.
2) RajKamal, “Mobile Computing”,OxfordUniversityPress,2007,
3) Prasant Kumar Pattnaik ,Rajib Mall,”Fundamentals of Mobile Computing”, PHI ,2012

18UECL702	CCN Laboratory	(0-0-2) 1

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on the process of data communication in computer network through the layered architecture. It also deals with the IEEE standards and various protocols at different layers.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Illustrate** the importance of High-Level Data Link Control.	-	1	4
CO-2	**Demonstrate** various functionalities Of Network Layer and usage of algorithms for routing strategies, packet management.	1,4	-	-

CO-3	**Demonstrate** the performance of various protocols and algorithms for Framing, Flow control, Error control and media access control	1,2	3,14	11
CO-4	**Illustrate** the various functionalities of RTOs.	-	3,14	1,2
CO-5	**Demonstrate** the usage and importance of Inter Process Communication(IPC)	2,3	14	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.25	2.23	2.23	2.0		-	-	-	-	-	1	-	-	2

Pre-requisites: Fundamentals of Computer Communication Networks Operating Systems, Knowledge of Embedded Systems.

CCN Experiments:

- Write a C program to simulate bit stuffing and de stuffing in data frames.
- Write a C program to simulate shortest path algorithm.
- Write a C program to implement Sliding Window protocol.
- Write a C program to implement Pipelining protocol which allows multiple outstanding frames.
- Write a C program to compute the polynomial cyclic redundancy check code (CRC Code checksum) for CRC-CCITT.
- Write a C program to simulate a positive acknowledgement with retransmission protocol.
- Write a C program for congestion control using leaky bucket algorithm.
- Write a C program for hamming code (error detection and error correction).

Embedded Experiments:

Note: Implement using RTOS Kernel either RTX, uCOS-II or Free RTOS on LPC2148 ARM-7 kit.

- OS concepts such as task management, IPC, Semaphore, Scheduling can also be demonstrated on Linux platform using gcc.

- Write a C program to create two tasks one to blink all LEDs with fixed delay, other to blink half of the LEDS (use task create, prioritize tasks, task delay and finally kill one of the task after certain delay).
- Demonstrate Producer and Consumer problem using semaphores.
- Demonstrate IPC using pipes and mailboxes.
- Create multiple tasks and demonstrate different scheduling algorithms (round robin, FIFO ,Preemptive).

Reference Books:

1) B. Forouzan, "Data Communication and Networking",4th Edition, TMH, 2006.
2)James F .Kurose, KeithW. Ross, "Computer Networks", Pearson education,2ndEdition, 2003.
3) Wayne Tomasi, "Introduction to Data communication and Networking", Pearson Education,2007.
4) James K. Peckol, "Embedded Systems–A contemporary Design Tool", John Weily, 2008.

18UECL703	Major Project Phase - I	(0-0-4) 2

Contact Hours: 52

Course Learning Objectives (CLOs):

The objectives of final year project during phase-I are to:

- Allow the students to demonstrate the skills learnt during their course of study by asking them to deliver a product that has passed through design, analysis, testing and evaluation stages.
- Encourage multidisciplinary research through the integration of material learnt in number of courses.
- Allow students to develop problem solving, analysis, synthesis and evaluation skills.
- Encourage teamwork and improve students' communication skills through project reports and presentations of their work.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** societal problems and analyze from engineering view point.	1,2	-	6,7

CO-2	**Perform** extensive literature survey on the identified problem and **explore** possible technical solutions.	1,2,3,4	5	13,14
CO-3	**Implement** and provide feasible solution for the identified problem.	1,2,3,4	5	13
CO-4	**Develop** presentation skills of summarizing technical contents and **organize** the study material in the form of a report.	10	11	-
CO-5	**Inculcate** professional ethics, moral responsibilities and develop the spirit of team work.	8,9	12	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	**3**	**3**	**3**	**3**	**2**	**1**	**1**	**3**	**3**	**3**	**2**	**2**	**1**	**1**

Major Project phase-I is a substantial piece of work that requires creative activity and original thinking. The project phase-I has to start with the problem formulation that will lead to feasible solutions. The material collection, survey, visits, data collection, preliminary design, analysis etc. is to be done in this phase. The project shall consist of a team of students not more than 4. Each batch shall be assigned with a guide. The guide will continuously monitor and evaluate the student project. Further, a review team will also evaluate the project progress.

18UECL704	**Internship**	**4 Weeks**

Course Learning Objectives (CLOs):

The students are to undergo internship in Private industries/R&D organizations/ Centres of Excellence/Laboratories of Reputed Institutions/Govt. & Semi Govt. organizations, PSUs, construction companies, entrepreneurial organizations, inter departments within the college etc. to get en exposure to the external world for a period of 4 weeks in the summer vacation after VI semester and before start of VII

semester. The students are to prepare a report on the internship work carried out. The internal faculty shall monitor the student and award CIE marks. There is a SEE in which the student shall present his work before a panel of examiners consisting of HoD, Guide and one faculty member during VII semester. The performance shall be communicated to the CoE office and the same shall reflect in the VII semester grade card.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Acquire** practical experience in an organizational setting	1,2	-	-
CO-2	**Apply** the knowledge and skill set in engineering design processes appropriate to the internship program.	1,2,3,4	5	-
CO-3	**Apply** modern tools and processes to solve the live problems.	5	3,4	-
CO-4	**Get** an opportunity to learn new skills	10	11	-
CO-5	**Learn** strategies like time management, multi-tasking, communication and team work skills in an industrial setup.	8,9	12	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	**3**	**3**	**2.5**	**2.5**	**2.5**	**-**	**-**	**3**	**3**	**3**	**2**	**2**	**-**	**-**

VIII Semester

18UECC800	Wireless Communication	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on evolution of wired Telecommunication, comparison of wireless1G, 2G, 3G, LTE,4G and 5G Networks, its advantages/ applications. It covers cellular structure, capacity expansion methods, modulation techniques with mathematical description for their parameters and its Hardware and IEEE standards with respect to 4G technology.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Discuss** the evolution and history of wireless technology and **compare** different mobile Networks along with their common System components.	-	3,4,5,13	1,2,10,12
CO-2	**Apply** the cellular concepts such as frequency reuse, handoff to **evaluate** the signal reception and Performance of cellular systems.	13	4,5,14	1,2,3,10, 12
CO-3	**Explain** the GSM techniques and its architecture with time slot structures and **study** different traffic case operations and protocol stack in GSM.	-	4,5	1,2,3,10, 12
CO-4	**Analyze** CDMA techniques with their channel structures and **scrutinize** future mobile communication networks.	-	5,6,7	1,2,3,4,10, 12
CO-5	**Describe** modulation techniques in wireless networks and **Explain** IEEE standards and protocols of Wireless networks	-	5,6,7	1,2,3,4,10, 12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	1	1.2	1.6	2	2	2	-	-	1	-	1	2.5	2

Pre-requisites: Analog Communication, Digital Communication
Contents:

Unit-I

Introduction to Wireless Communication: Introduction to wireless communication systems and networks, history and evolution, different generations of wireless cellular networks, 1G, 2G, 3G and 4G networks.
Cellular System: Common cellular system components, common cellular network components, hardware and software, views of cellular networks, 3G cellular systems components, and cellular component identification call establishment.
12 Hrs

Unit-II

Cellular structure and fundamentals: Wireless network architecture and operation, cellular concept, cell fundamentals, capacity expansion techniques, mobility management, radio sources and power management, wireless network security, SS7. **09 Hrs**

Unit-III

Second Generation mobile system: GSM and TDMA techniques, GSM system, overview, GSM network and system architecture, GSM channel classifications & concepts, GSM identifiers.
GSM system operation: System Operation traffic cases, call handoff, roaming, GSM protocol architecture, TDMA systems. **12 Hrs**

Unit-IV

Third, Fourth and Fifth Generation mobile system: CDMA technology CDMA overview, CDMA channel concept, CDMA operations. LTE and 4G architectures and their comparisons, Introduction to 5G and its features. **9 Hrs**

Unit-V

Modulation Techniques: Wireless modulation techniques and hardware, characteristics of air interface, path loss models, wireless coding techniques, digital modulation techniques, OFDM, UWB radio techniques, diversity techniques, demonstration of typical GSM, CDMA hardware.
IEEE standards: Introduction to wireless LAN, 802.11X technologies, introduction to 802.15X, technologies in PAN applications, Introduction to Bluetooth model, introduction to broadband wireless MAN, 802.16X technologies, Black Berry Handsets. **10 Hrs**

Activity beyond Syllabus:
BSNL exchange visit

Reference Books:

1) Mullet,"Wireless Telecommunication Systems and networks", Thomson Learning 2006.
2) Lee W.C.Y," Mobile Cellular Telecommunication",MGH,2002.
3) D.P. Agrawal," Wireless communication",2/e, Thomson Learning,2007.
4) T.S. Rappaport," Wireless Communications", principles &practice, 3/e, Pearson Education,2008.

18UECE810 Adhoc Wireless networks (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on functions and protocols of Adhoc Wireless Networks.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** typical issues in ad-hoc/sensor networks and **Analyze** the challenges in designing MAC protocols	-	13	1,2
CO-2	**Classify** MAC protocols and **investigate** the challenges in designing routing protocols and classify them for ad-hoc wireless networks.	1,2,13	3	4
CO-3	**Discuss** the challenges in designing transport layer protocols for wireless ad-hoc/sensor networks.	1,2,13	3	
CO-4	**Describe** security issues for wireless ad-hoc networks.		1,2,3,13	
CO-5	**Analyze and compare** different routing protocols in network layer and protocols for process to process delivery of information in transport layer.	-	3,13	1,2,5,12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2	2	2	1	1	-	-	-	-	-	-	1	2.4	

Prerequisites:

Computer Communication Networks, Basic Wireless Communication Concepts.

Contents:

Unit-I

Adhoc Networks: Introduction, Issues in Ad hoc wireless networks, Ad hoc wireless internet.

MAC Protocols For Ad Hoc Wireless Networks: Introduction, Issues in designing a MAC protocol for Ad hoc wireless Networks, Design goals of a MAC protocol for Ad hoc wireless Networks. 0**8Hrs**

Unit-II

Classification of MAC protocols: Contention - based MAC protocols with scheduling mechanism, MAC protocols that use directional antennas, Other MAC protocols.

Routing Protocols for Ad Hoc Wireless Networks: Introduction, Issues in designing a routing protocol for Ad hoc wireless Networks, Classification of routing protocols,Table driven routing protocol, On-demand routing protocol, Hybrid routing protocol, Routing protocols with effective flooding mechanisms, Hierarchical routing protocols, Power aware routing protocols.

08 Hrs

Unit-III

Transport Layer Protocols For Ad Hoc Wireless Networks: Introduction, Issues in designing a transport layer protocol for Ad hoc wireless Networks, Design goals of a transport layer protocol for Ad hoc wireless Networks. **08 Hrs**

Unit-IV

Security: Security in wireless Ad hoc wireless Networks, Network security requirements, Issues & challenges in security provisioning. **08 Hrs**

Unit-V

Quality Of Service In Ad Hoc Wireless Networks: Introduction, Issues and challenges in providing QoS in Ad hoc wireless Networks, Classification of QoSsolutions 0**7 Hrs**

Reference Books:

1) C. Siva Ram Murthy & B. S. Manoj, Adhoc wireless Networks, Pearson Education, 2nd Edition, reprint 2005.

2) Ozan K. Tonguz and Gianguigi Ferrari, Adhoc wireless Networks, Wiley Publications, 2009.

3) Cheng, Xiao Hung, Ding- Zhu Du, Kluwer, Adhoc wireless Networking, Xiuzhen Academic publishers, 2013.

4) B. S. Manoj and C. Siva Ram Murthy, Ad Hoc Wireless Networks: Architectures and Protocols, 6th Edition, Pearson Education, 2008.

18UECE811	Reconfigurable Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on key criteria: area, speed, optimization techniques employed, various system architectures considered in the FPGA method of Design.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** the basics of FPGA Architecture and its Function mapping.	-	1,2	13,14
CO-2	**Modeling** the languages and its synthesis.	-	1,2	-
CO-3	**Understand** AdvancedFPGA design principles w.r.t speed and area.	1,2	-	-
CO-4	**Design** strategies for DSP and Image Processing applications.	3	13,14	5
CO-5	**Analyze** and **explore** the architectural design of FPGA for Deep Learning Applications.	3	13,14	5

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.33	2.33	3	-	1	-	-	-	-	-	-	-	1.66	1.66

Pre-requisites: Knowledge of FPGA and microcontroller architecture

Contents:

Unit-I

FPGA Design Flow: Reconfigurable Logic Devices, Field-Programmable Gate Arrays, Basic Architecture, Example Actel Devices: ACT1 logic module, Shannon's expansion theorem, Routing, Programmable I/O Architectures**,** Specialized Function Blocks: Embedded Microprocessors. Coarse-Grained Reconfigurable Arrays: Raw &PipeRench Architectures. **6 Hrs**

Unit-II

Languages and Compilation, Design Cycle, Languages, Algorithmic RC Languages, Hardware Description Languages (HDL): Modelling of Abstraction Level, High Level Compilation, Compiler Phases. Analysis and Optimizations, Scheduling, Low Level Design Flow, Logic Synthesis Technology Mapping, Logic Placement, Signal Routing Configuration Bit streams **8Hrs**

Unit-III

Architecting Speed & Area Speed: High Throughput, Low Latency, Timing, Add Register Layers, Parallel Structures, Flatten Logic Structures, Register Balancing, Reorder Paths.**Area:**Rolling Up the Pipeline, Control-Based Logic Reuse, Resource Sharing, Impact of Reset on Area, Resources Without Reset, Resources Without Set, Resources Without Asynchronous Reset, Resetting RAM, Utilizing Set/Reset FF Pins. **8 Hrs**

Unit-IV

FPGA Applications: Signal processing applications: Filtering, DSP application building blocks: Efficient Airthmetic, CORDIC, Transforms, Examples: Beam forming, Software Defined Radio. **Image and video processing**: Local Neighbourhood functions, Convolution, Morphological Operations, Feature Extraction & matching. **8 Hrs**

Unit-V

Accelerating the CNN Inference on FPGAs : Introduction, Background on CNNs and Their Computational Workload, General Overview, Inference versus Training, Inference, Layers, and CNN Models, FPGA-Based Deep Learning Computational Transforms: Winograd Transform and Fast Fourier Transform, Loop Unrolling. Loop Tiling. **Approximate Computing of CNN Models**: Approximate Arithmetic for CNNs, Fixed-Point Arithmetic, Dynamic Fixed Point for CNNs, FPGA

Implementations, Extreme Quantization and Binary Networks, Reduced Computations, Weight Pruning, Low Rank Approximation. **9 Hrs**

Activity Beyond Syllabus: Seminar on Reconfigurable Computing.

Reference Books:

1) M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
2) Steve Kilts,” Advanced FPGA Design Architecture, Implementation, and Optimization”, WILEY INTERSCIENCE, 2007.
3) Mahmoud Hassaballah and Ali Ismail Awad, “Deep Learning inComputer Vision”, CRC Press,Taylor& Francis Group, 2020.
4) Deep Learning by Ian Goodfellow and YoshuaBengio and Aaron Courville, MIT Press.https://www.deeplearningbook.org/

18UECE812 Low Power VLSI Design (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on factors which may lead to the techniques of power saving in design of VLSI circuits. Knowledge of CMOS digital circuits and analog Mixed Mode VLSI Design are required as prerequisites.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**List** the factors effecting the power requirement in design of VLSI circuits.	-	-	2,3,13
CO-2	**Explain** various methods of achieving the power minimization	2,13	-	-
CO-3	**Compare** various methods of achieving the power minimization	1,2,12	-	-
CO-4	**Estimate** the features of synthesis tools for Low Power VLSI Design	-	5	-
CO-5	**Analyze**and **investigate** switched capacitance, leakage power minimization techniques	1,2	4	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	2.5	1	2	2	-	-	-	-	-	-	3	2	-

Prerequisites: Basics of CMOS digital circuits and Analog Mixed Mode Design.

Contents:

Unit-I

MOS Transistor structure and device modeling, MOS Inverters, MOS Combinational Circuits - Different Logic Families. **08 Hrs**

Unit-II

Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom

Supply Voltage Scaling Approaches: Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management. **08 Hrs**

Unit-III

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff, Bus Encoding, Two's complement Vs Sign Magnitude, Architectural optimization, Clock Gating, Logic styles. **08 Hrs**

Unit-IV

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS). **08 Hrs**

Unit-V

Special Topics: Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design, CAD tools for low power synthesis. **07 Hrs**

Reference Books:

1) Gary K Yeap, "Practical low power digital VLSI Design" ,Kluwer Academic, 1998.
2) Jan M. Rabaey, MassoudPedram, " Low power design methodologies", Kluwer

Academic, 2010.
3)Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, Wiley 2000.
4) A.P. Chandrasekaran and R. W. Broadersen, “Low power digital CMOS design”, Kluwer Academic, 1995.

18UECE813	Digital Signal Compression	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the need of compression, various lossless and lossy compression techniques and their performance measures.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the need, types and the mathematical preliminaries required for compression	-	1	-
CO-2	**Analyze** different lossless coding techniques for uncorrelated sources	-	2,3	4,5
CO-3	**Analyze** different lossless coding techniques for correlated sources	-	2,3	4,5
CO-4	**Understand** and **Analyze** various scalar quantization techniques for lossy compression	-	2,3	4,5
CO-5	**Understand** and **Analyze various** vector quantization techniques for lossy compression	-	2,3	4,5

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2	2	2	1	1	-	-	-	-	-	-	-	-	-

Pre-requisites: Digital Signal Processing, Digital Communication, Information Theory and Coding.

Contents:

Unit-I

Introduction: Compression techniques: Lossless Compression, Lossy Compression, Measure of performance, Modeling & coding.

Mathematical Preliminaries for Lossless Compression: A brief introduction to information theory, Models: Physical models, Probability models, Markov models, composite source model, Coding: uniquely decodable codes, Prefix codes.

Mathematical Preliminaries for Lossy Compression: Introduction, Distortion Criteria, Models: Probability models, Linear System Models, Physical models.

08 Hrs

Unit-II

Huffman coding: Minimum variance Huffman codes, Adaptive Huffman coding: Update procedure, Encoding procedure, Decoding procedure. Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding: Lossless image compression, Text compression, Audio Compression. **08 Hrs**

Unit-III

Arithmetic Coding: Coding a sequence, Generating a Tag, Deciphering the Tag, Generating a binary code: Uniqueness and Efficiency of the Arithmetic Code, Algorithm Implementation, Integer Implementation, Comparison of Binary and Huffman coding, Applications.

Dictionary Techniques: Introduction, Static Dictionary: Diagram Coding, Adaptive Dictionary: The LZ77 Approach, The LZ78 Approach, Applications. **08 Hrs**

Unit-IV

Scalar Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization: Forward Adaptive Quantization, Backward Adaptive Quantization, Non-uniform Quantization: pdf optimized Quantization, Compaded Quantization.

08 Hrs

Unit-V

Vector Quantization: LBG algorithm, Tree structured VQ, Structured VQ, Trellis coded quantization. **07 Hrs**

Reference Books:

1) K. Sayood, “Introduction to Data Compression," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.

2) N. Jayant and P. Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video,” Prentice Hall, USA, 1984.
3) D. Salomon, “Data Compression: The Complete Reference”, Springer, 2000.
4) Z. Li and M.S. Drew**,** “Fundamentals of Multimedia,” Pearson Education (Asia) Pvt. Ltd., 2004.

18UECO820	**DSP Architecture**	**(3-0-0)3**

Contact Hours: 39

Course Learning Objectives (CLOs):

Digital Signal Processor Architecture focuses on various architectural requirements and concepts of a digital signal processor, programming aspects and interfacing the processor to memory and I/O devices considering as exampleTMS320C54xx.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** basics of DSP, Computational Accuracyin a digital signal processor.	-	1	-
CO-2	**Describe** architectural featuresof a digital signal processor.	-	3,5	-
CO-3	**Describe** Instructions and Programming aspects of a digital signal processor.	-	3,5	12
CO-4	**Implement** DSP Algorithms and **develop** programmingskills for signal processing.	-	3, 12	-
CO-5	**Interface** Memory And Parallel I/O Peripherals digital signal processor.	-	13	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2	-	2	-	2	-	-	-	-	-	-	1.5	2	-

Prerequisites: Digital Signal Processing

Contents:

Unit-I

Introduction To Digital Signal Processing: Introduction, A digital signal processing system, the sampling process, discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), LTI systems, Digital filters.

Computational Accuracy in DSP Implementation: Introduction, Number formats for signals and coefficients in DSP systems, Dynamic range and precision, Sources of error in DSP implementations, A/D conversion error, DSP computational error and D/A Conversion error. **08Hrs**

Unit-II

Digital Signal Processing Devices: Introduction, Basic architectural features, DSP computational building blocks, Bus architecture and memory, Data addressing capabilities, Address generation unit, Programmability and Program execution, Speed issues.

Programmable Digital Signal Processors: Introduction, Architecture of TMS320C54xx digital signal processors: Bus structure, Central processing unit, internal memory and memory mapped registers, Data addressing modes of TMS320C54xx processors, Memory space of TMS320C54xx processors. **08Hrs**

Unit-III

TMS320C54xx Instructions and Programming, On-chip peripherals, Interrupts of TMS320C54xx processors, Pipeline operation of TMS320C54xx processors. **07Hrs**

Unit-IV

Implementation Of Basic DSP Algorithms: Introduction, The Q-notation, Linear Convolution, Circular Convolution, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, butterfly computation and FFT implementation on the TMS320C54xx. **08Hrs**

Unit-V

Interfacing Memory And Parallel I/O Peripherals To Programmable DSP Devices: Introduction, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access(DMA). Interfacing Serial Converters to a Programmable DSP device: Introduction, Synchronous Serial Interface (SSI), A multi channels buffered serial port (McBSP). **08 Hrs**

Reference Books:

1) Avtar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Publications, 2004.
2) Lapsley et al. DSP Processor Fundamentals, Architectures & Features"S. Chand & Co, 2000.
3) B.VenkataRamani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2004.

18UECO821	CAD for VLSI	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on key criteria in VLSI CAD such as basic data structures and algorithms, partitioning, floor planning, placement and routing. Various algorithms that are used for constructing the CAD tools are discussed.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Comprehend** the basic algorithms required for VLSI CAD.	-	2,4	1
CO-2	**Recognize** the basic data structures and graph algorithms for physical design issues.	-	2,3	4
CO-3	**Sequence** various operations in partitioning and floor planning.	-	2	-
CO-4	**Recognize** the various challenges in pin assignment and placement phases.	-	-	5
CO-5	**Evaluate** the global and detailed routing methods.	12	5	13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	2	2	1.5	1.5	-	-	-	-	-	-	3	1	-

Pre-requisites: VLSI Basics

Contents:

Unit-I

Basic Algorithms: Basic terminology, Complexity issues and NP-Hardness. Examples - Exponential, heuristic, approximation and special cases. Basic Algorithms. Graph Algorithms for Search, spanning tree, shortest path, min-cut and max-cut, Steiner tree. Computational Geometry Algorithms: Line sweep and extended line sweep methods. **08Hrs**

Unit-II

Basic Data Structures: Atomic operations for layout editors, linked list of blocks, Bin-based method, Neighbor pointers, corner-stitching, multi-layer operations, Limitations of existing data structures. Layout specification languages.

Graph algorithms for physical design: Classes of graphs in physical design, Relationship between graph classes, Graph problems in physical design, Algorithms for Interval graphs, permutation graphs and circle graphs. **08Hrs**

Unit-III

Partitioning: Problem formulation, Design style specific partitioning problems, Classification of Partitioning Algorithms. Group migration algorithms: Kernighan-Lin algorithm, Fiduccia-Mattheyses Algorithm, Simulated Annealing, Simulated Evolution.

Floor Planning: Problem formulation, Constraint based floor planning, Rectangular dualization, Simulated evolution algorithms. **08Hrs**

Unit-IV

Pin Assignment: Problem formulation. Classification of pin assignment problems, General pin assignment problem.

Placement: Problem formulation, Classification of placement algorithms. Simulation based placement: Simulated annealing, simulated evolution, force directed placement. Partitioning based algorithms: Breur‘s Algorithm, Terminal propagation algorithm, Other algorithms for placement. **08 Hrs**

Unit-V

Global Routing: Problem formulation, Classification of Global routing algorithms, Maze routing algorithms: Lee‘s algorithm, Soukup‘s algorithm and Hadlock‘s Algorithm, Line probe algorithms.

Detailed Routing: Problem formulation, Routing considerations, models, channel routing and switch box routing problems. General river routing problem, Single row routing problem. Two-layer channel routing algorithms: Basic Left Edge Algorithm, Dogleg router, Symbolic router-YACR2. **07Hrs**

Reference Books:

1) Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Ed, 1999 Kluwer Academic Publishers, Reprint 2013 Springer (India) Private Ltd. ISBN 978-1475771947.
2) Rolf Drechsler, "Evolutionary Algorithms for VLSI CAD", Springer reprint, 2010, ISBN-13 : 978-1441950406.
3) Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011, ISBN-13 : 978-9048195909.
4) Niranjan N. Chiplunkar, Kotari Manjunath, "VLSI CAD", PHI Publication, 2011.

18UECO822	**Operations Research**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

This course aims to introduce students to use quantitative methods and techniques for effective decisions–making; model formulation and applications that are used in solving business decision problems.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Recognize** the need for operation research.	-	2,4	1
CO-2	**Design** the alternative solutions for transportation problem.	-	2,3	4
CO-3	**Sequence** various operations in an establishment.	-	2	-
CO-4	**To comprehend** the characteristics of different types of decision-making environments and the appropriate decision making approaches and tools to be used in each type.	-	-	5

CO-5	**Evaluate** various inventory control techniques and device the CPM and PERT methods for project management.	12	5	13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	2	2	1.5	1.5	-	-	-	-	-	-	3	1	-

Pre-requisites: Management & Entrepreneurship, Basics of Statistics

Contents:

Unit-I

Introduction to OR: Basics definition, scope, objectives, phases, models and limitations of Operations Research.

Linear Programming Problem: Formulation of LPP, Graphical solution of LPP, Simplex Method, Artificial variables, big-M method. **08Hrs**

Unit-II

Transportation Problem: Formulation, solution, unbalanced Transportation problem. Finding basic feasible solutions – Northwest corner rule, least cost method and Vogel's approximation method.

Assignment Model: Formulation, Hungarian method for optimal solution Solving unbalanced problem, Traveling salesman problem and assignment problem.**08Hrs**

Unit-III

Sequencing models Solution of Sequencing Problem – Processing n Jobs through 2 Machines – Processing n Jobs through 3 Machines – Processing 2 Jobs through m machines – Processing n Jobs through m Machines.

Decision theory Decision under uncertainty, Decision under certainty, Decision under risk, Decision trees, Game Theory, Two-person zero sum game, Competitive games. **08Hrs**

Unit-IV

Game Theory Two-person zero sum game, Competitive games, rectangular game, saddle point, mini-max (maximin) method of optimal strategies, value of the game.

Replacement Models Replacement of Items that Deteriorate whose maintenance costs increase with time without change in the money value, Replacement of items that fail suddenly: individual replacement policy, group replacement policy. **08 Hrs**

Unit-V

Inventory Models Inventory costs, Models with deterministic demand – model (a) demand rate uniform and production rate infinite, model (b) demand rate non-

uniform and production rate infinite, model (c) demand rate uniform and production rate finite.

Project Management Phases of project management, guide lines for network construction, CPM and PERT, Resource analysis in network scheduling, updating a project. **07Hrs**

Reference Books:

1) A M Natarajan, P. Balasubramani,"Operation Research", 2nd Edition, Pearson Publications, 2014.
2) J.K. Sharma, "Operation Research : Theory and applications", 5th Edition, Macin Publishers, 2012.
3) Wayne L Winston,"Operations Research : Applications and Algorithms", Duxbuty Press, 2003.
4) Hamdy H Taha, "Operations Research : An Introduction", 9th Edition, Pearson Education, 2010.

18UECO823	Advanced Computer Architecture	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course deals with the understanding quantitative principles guiding the computer system design. It focuses on enhancing the performance by addressing parallelism at different levels such as Instruction, thread, task, job. Evaluates memory hierarchy, speculations, ISA, ALU architectures, choice of I/O is major motivation.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** the performance, Quantitative Principles of computer design and Choose/utilize Computer Arithmetic units.	1,2	3,4	-
CO-2	**Identify and address** concepts and challenges of ILP	1, 2	3	4

CO-3	**Investigate** Hardware and Software for VLIW and EPIC	-	1,2,3	5
CO-4	**Design** and **evaluating** an I/O system	1,3	-	5
CO-5	**Comprehend** Critical Performance Issue and **deduce** Characteristics of Scientific Applications	2	4,6	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.75	2.75	2.25	1.67	1	2	-	-	-	-	-	-	-	-

Pre-requisites:

Knowledge of Processor/Controllers, Languages-Compilers is appreciated.

Contents:

Unit-I

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design

Some topics in Pipelining: Instruction –Level Parallelism, Its Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls. **7 Hrs**

Unit-II

Introduction to limits in ILP: Performance and efficiency in advanced multiple-issue processors.

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy. Fallacies and pitfalls in the design of memory hierarchies. **8 Hrs**

Unit-III

I/O performance: reliability measures, and benchmarks; Queuing theory; Crosscutting issues; Designing and evaluating an I/O system –The Internet archive cluster

Hardware and Software for VLIW: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop- Level Parallelism, Scheduling and Structuring Code for Parallelism. **8 Hrs**

Unit-IV

EPIC Introduction and Large-Scale Multiprocessors : Hardware Support for Exposing Parallelism: Predicated Instructions, Hardware Support for Compiler

Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks.Introduction, Inter-processor Communication: The Critical Performance Issue. **8 Hrs**

Unit-V

Scientific Applications and Computer Arithmetic: Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications, Implementing Cache Coherence, The Custom Cluster Approach: Blue Gene/L, Concluding Remarks, Introduction, Basic Techniques of Integer Arithmetic, Floating Point, Floating-Point Multiplication, Floating-Point Addition. **8 Hrs**

Reference Books:

1) Kai Hwang, "Advanced Computer Architecture - Parallelism, Scalability, Programmability", 2nd Edition.
2) Computer architecture, Pipelined and parallel Processor Design', M.J.Flynn, Narosa Publishing,2002.
3) Hennessey and Patterson, "Computer Architecture A Quantitative Approach", 4th Edition, Elsevier, 2007.
4) 'An introduction to parallel computing : Design and Analysis of Algorithms', Ananth Grama,Pearson,2nd Edition,2004.

18UECL801	**Technical Seminar**	**(3-0-0) 3**

Contact Hours: 26

Course Learning Objectives (CLOs):

The objective of seminar is to prepare the students for independent study of the state of the art topics in the broad areas of interest. The students are exposed to various aspects of seminar such as literature survey, organization of the material, technical writing and presentation skills.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Read and Understand** technical topics from technical journals/ magazines.	-	1,2	6,7,12
CO-2	**Analyze** technical content and extract necessary information.	1,2	-	-
CO-3	**Organize** the topic in a systematic manner and **prepare** the report in a specific format	-	5	-

CO-4	**Present** the topic in a convincing manner	9,10	-	13
CO-5	**Inculcate** professional ethics and moral responsibilities	8	-	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.5	2.5	-	-	-	1	1	3	3	3	-	1	1	-

Technical Seminar: The students are expected to learn how to carry out literature survey to locate the state of the art technology in engineering domain of their interest. They are required to carry out selection of an emerging topic beyond the syllabus relevant to the branch of study, understand the concept, analyze and present effectively for 15-20 minutes followed by 5 minutes of questions and answers before their classmates and faculty. They can also present the technical innovative/novel work carried out in the laboratory. Students are also required to learn the effective communication and modalities of technical interactions. Further, they have to submit the seminar material in the form of a paper in IEEE format. All the students are required to attend all the sessions throughout the semester.

18UECL802 Project Phase – II (0-0-12) 7

Contact Hours: 100

Course Learning Objectives (CLOs):

The objectives of final year project are to:

- Allow students to demonstrate wide range of skills learned during their course of study by asking them to deliver a product that has passed through the design, analysis, testing and evaluation stages.
- Encourage multidisciplinary research through the integration of material learned in a number of courses.
- Allow students to develop problem solving, analysis, synthesis and evaluation skills.
- Encourage teamwork.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Arrive** at an optimal solution towards the problem identified	1,2,3,9	4	5,12

CO-2	**Implement** proposed solution in the form of development of software and/ or hardware prototype.	3,4,9,13, 14	5,6,7	12
CO-3	**Organize** the topics in a systematic manner and **prepare** report in a specific format	9,10,11	-	12
CO-4	**Present** the work in a systematic way	-	1,6,10	-
CO-5	**Adopt** professional ethics and responsibilities	8	11,12	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	3	3	2.5	1	2	2	3	3	2.5	2.5	1.3	3	3

Major Project phase-II is the continuation from phase – I in which the students are expected to go for material collection, survey, visits, data collection, optimized design, analysis, model development, code writing, field work etc. The same project team formed for phase –I will continue the work under the guidance of the same faculty member. For all the projects, problems may be domain specific or interdisciplinary in nature. The guide will continuously monitor and evaluate the student project. Further, a review team will rigorously evaluate the project progress and completion.