Academic Program: UG

Academic Year 2023-24

Syllabus

V & VI Semester B.E.

Electronics & Communication Engineering

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

Accredited by NBA under Tier-1 2023-2026

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for V &VI semester of UG program in Electronics and Communication Engineering is recommended by Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2023-24 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College – Vision and Mission

VISION:

To develop competent professionals with human values

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department- Vision and Mission

Vision

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

Mission

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, effective teaching learning process and the best of laboratory facilities.

M2: To encourage innovation, research culture and team work among students.

M3: Interact and work closely with industries and research organizations to accomplish knowledge at par.

M4: To train the students for attaining leadership with ethical values in developing and applying technology for the betterment of society and sustaining the global environment.

Program Educational Objectives (PEOs)

The Graduates, after a few years of Graduation will be able to:

I. **Apply** the latest in-depth knowledge in the field of Electronics and Communication Engineering with Mathematical applications to address real life challenges.
II. **Exhibit** the confidence for independent working and / or spirit to work cohesively with group.
III. **Readily** be accepted by the Industry globally.
IV. **Develop** design skills, fault diagnosis skills, communication skills and create research orientation.
V. **Inculcate** professional, social ethics and to possess awareness regarding societal responsibility, moral and safety related issues

Programme Outcomes (POs):

Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

13. Design economically and technically sound analog and / or digital systems based on the principles of signal processing, VLSI and communication Engineering (PO-13)

14. Integrate hardware – software, and apply programming practices to realize the solutions in electronics domain. (PO-14)

SDM COLLEGE OF ENGINEERING AND TECHNOLOGY, DHARWAD
Department of Electronics and Communication Engineering
V Semester
Scheme of Teaching and Examinations 2023 – 24

Course Code	Course Category	Course Title	Teaching		Examination				
			L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
					Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration in Hrs.
21UHUC550	HU	Management, Entrepreneurship and IPR	3 - 0 - 0	3	50	100	3	-	-
21UECC500	PC	CMOS VLSI Design	3 - 0 - 0	3	50	100	3	-	-
21UECC501	PC	Microwave and Antennas	2 - 2 - 0	3	50	100	3	-	-
21UECC502	PC	Object Oriented Programming using C++	3 - 0 - 0	3	50	100	3	-	-
21UECE55X	PE	Program Elective – 1	3 - 0 - 0	3	50	100	3	-	-
21UECL504	PC	Communication Systems Laboratory	0 - 0 - 2	1	50	--	--	50	3
21UECL505	PC	Object Oriented Programming using C++ Laboratory	0 - 0 - 2	1	50	--	--	50	3
21UAEE55X	AE	Ability Enhancement Course	2 - 0 - 0	2	50	50	2	--	--
21UECL506	PC	Minor Project - I	0 - 0 - 2	1	50	--	--	--	--
21UECL507	PC	Internship -I	Two weeks	1	50	--	--	--	--
		Total	**16 - 2 - 6**	**21**	**500**	**550**		**100**	
Program Elective-1									
21UECE551	PE	Operating Systems	3 - 0 - 0	3	50	100	3	-	-
21UECE552	PE	IoT and Applications	3 - 0 - 0	3	50	100	3	-	-
21UECE553	PE	Automotive Electronics	3 - 0 - 0	3	50	100	3	-	-
Ability Enhancement Course									
21UAEE550	AE	System Verilog	2 - 0 - 0	2	50	50	2	--	--
21UAEE551	AE	Python Programming	2 - 0 - 0	2	50	50	2	--	--

PC- Program Core, PE-Program Elective, OE- Open Elective and HU- Humanities. **CIE**: Continuous Internal Evaluation **SEE**: Semester End Examination **L**: Lecture **T**: Tutorials **P**: Practical *SEE for theory courses is conducted for 100 marks and reduced to 50 marks

SDM COLLEGE OF ENGINEERING AND TECHNOLOGY, DHARWAD
Department of Electronics and Communication Engineering
VI Semester
Scheme of Teaching and Examinations 2023 – 24

Course Code	Course Category	Course Title	Teaching		Examination				
			L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
					Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration In Hrs.
21UECC600	PC	Analog & Mixed Mode VLSI Design	3 - 0 - 0	3	50	100	3	-	-
21UECC601	PC	Embedded Systems	3 - 0 - 0	3	50	100	3	-	-
21UECC602	PC	Computer Communication Networks	3 - 0 - 0	3	50	100	3	-	-
21UECE65X	PE	Program Elective -2	3 - 0 - 0	3	50	100	3	-	-
21UECE65X	PE	Program Elective - 3	3 - 0 - 0	3	50	100	3	-	-
21UECO65X	OE	Open Elective - 1	3 - 0 - 0	3	50	100	3	--	--
21UECL603	PC	VLSI Laboratory	0 - 0 - 2	1	50	--	--	50	3
21UECL604	PC	Embedded Systems Laboratory	0 - 0 - 2	1	50	--	--	50	3
21UECL605	PC	Minor Project-II	0 - 0 -2	1	50	--	--	50	3
21UHUL606	HU	Soft skills/Aptitude	0 - 0 -2	1	50	--	--	--	--
		Total	**18 – 0 - 8**	**22**	**500**	**600**		**150**	
Program Elective -2									
21UECE651	PE	Digital Image processing	3 - 0 - 0	3	50	100	3	-	-
21UECE652	PE	Data Structures using C++	3 - 0 - 0	3	50	100	3	-	-
21UECE653	PE	Reconfigurable Design	3 - 0 - 0	3	50	100	3	-	-
21UECE654	PE	Cloud Computing	3 - 0 - 0	3	50	100	3	-	-
Program Elective - 3									
21UECE655	PE	Artificial Intelligence and Machine Learning	3 - 0 - 0	3	50	100	3	-	-
21UECE656	PE	Information Theory and Coding	3 - 0 - 0	3	50	100	3	-	-
21UECE657	PE	Nano Electronics	3 - 0 - 0	3	50	100	3	-	-
Open Elective – 1 (For All Branches)									
21UECO651	OE	Data Compression	3 - 0 - 0	3	50	100	3	--	--
21UECO652	OE	Cryptography	3 - 0 - 0	3	50	100	3	--	--
21UECO653	OE	Electronics in Automobile	3 - 0 - 0	3	50	100	3	--	--

V Semester

21UHUC550	Management, Entrepreneurship and IPR	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on concepts of Entrepreneurship, concepts of Management and about the Intellectual Property Rights. Entrepreneurship part discusses about meaning of Entrepreneurship, Business ideas, family business and doing business in India. Management part discusses about Planning, Forecasting, Organizing & Staffing, Motivating and Controlling. Intellectual Property Rights part discusses various legal aspects of Patents, Trademarks and Copyright.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the concept of Entrepreneurship and Business ideas.	12	6	-
CO-2	**Describe** about family business in India and doing business in India	12	6	-
CO-3	**Discuss** Management principles/process and illustrate Planning and Organizing.	-	11	-
CO-4	**Analyse** aspects of Motivating and Controlling functions of Management.	-	6	-
CO-5	**Discuss** about the legal aspects of Intellectual Property Rights: Patents, Trade Marks and Copyright.	8	12	7

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	-	-	-	-	-	2.0	1.0	3.0	-	-	2.0	2.7	**-**	**-**

Contents:

Unit-I

Entrepreneurship

Understanding Entrepreneurship: Introduction, Definition, Role of an Entrepreneur, Reasons for growth of Entrepreneurship, Age of an Entrepreneurial firm, Why start a business, Entrepreneurial Characteristics & Skills, Types of Entrepreneurs, Entrepreneurial failure.

Growth of a Business Idea: Introduction, New Business Idea, Pre-selection process, Sources of Business Ideas, Preliminary Research, Business Idea Evaluation.

Family Business: Introduction, Family Business in India, The Founder, The Next Generation, Entry of Family Members, Non-family Managers, Succession, Best Practices. **08 Hrs**

Unit-II

Doing Business in India: Introduction, Major Issues, Types of Organizations, Legal Compliances.

Entrepreneurial Support: Policies, Business Incubation, Business Clusters.

Management Planning, Forecasting and Decision Making: Nature of Planning, the foundation of planning, some planning concepts, forecasting, nature of decision making, management science, tools for decision-making. **08 Hrs**

Unit-III

Organizing and staffing: Nature of organizing, traditional organizational theory, technology and modern organization structures, staffing technical organization, authority and power; delegation, meeting & committees.

Motivating: Motivation, leadership, motivating and leading technical professionals.

Controlling: Process of control, financial controls, & non-financial controls. **07 Hrs**

Unit-IV

Intellectual Property Rights

Patents: Introduction, Protectable Subject Matter-Patentable Invention, Procedure for Obtaining Patent, Provisional and Complete Specification, Rights conferred on a Patentee, Transfer of Patent, Revocation and Surrender of Patents, Infringement of Patents. **08 Hrs**

Unit-V

Trade Marks: Introduction, Statutory Authorities, Principles of Registration of Trade Marks, Rights conferred by Registration of Trade Marks, Infringement of Trade Marks and Action against Infringement, Procedure of Registration and Duration.

Copyright: Introduction, Author and Ownership of Copyright, Rights conferred by Copyright, Term of Copyright, Assignment/License of Copyright, Infringement of Copyright, Infringement in Literary, Dramatic and Musical Works. **08 Hrs**

Reference Books:

1) Rajeev Roy, “Entrepreneurship”, 2nd Edition, 2011, Oxford University Press, New Delhi.
2) Daniel L Babcock, Lucy C Morse, "Managing Engineering and Technology" Third Edition, 2005, Prentice Hall of India Pvt. Ltd., New Delhi.
3) Wadehra B. L.,"Law relating to Intellectual Property”,4th Edition, 2012, Universal Law Publishing Co. Pvt. Ltd., Delhi.

4) N. K. Acharya, "Text book on Intellectual Property Rights" Asia Law House, Hyderabad, 4th Edition.

21UECC500	CMOS VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the theory, fabrication and design principles of CMOS devices and circuits. The course concentrates on the study and analysis of various combinational and sequential MOS logic circuits for digital VLSI applications.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction and the characteristics of MOS structures and logic circuits.	-	-	1,2,13
CO-2	**Elaborate** the steps and processes involved in the VLSI fabrication technology.	-	-	1,2,4
CO-3	**Apply** design rules to design layout of various digital VLSI circuits.	5	1,2	3,9
CO-4	**Estimate** the parasitics for various MOS layouts.	-	1	2
CO-5	Perform a **comparative** study of different MOS circuit technologies.	2	4,13	1,5,9

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.4	1.6	1	1.5	2	-	-	-	1	-	-	-	1.5	-

Pre-requisites:

Semiconductor Devices, Analog Electronic circuits, Digital Electronic circuits

Contents:

Unit-I

MOS Transistor: Metal Oxide Semiconductor (MOS) Structure, MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

MOS Inverters: Static Characteristics: Introduction, Resistive-Load Inverter, CMOS Inverter **08 Hrs**

Unit-II

Fabrication Technology: Introduction, Czochralski growth process, Fabrication processes: Thermal oxidation, Diffusion, Ion implantation, Photo lithography, Epitaxy, Metallization and interconnections, Ohmic and Schottky contacts, fabrication of resistors and capacitors.

Basic CMOS Technology: Basic CMOS technology: P-Well / N-Well / Twin Well process, MOS mask layer, stick diagrams, Lambda based design rules, Schematic and Layouts **08 Hrs**

Unit-III

Basic Circuit Concepts: Sheet resistance, standard unit capacitance, concepts delay unit time, Inverter delays, driving capacitive loads, Propagation delays, PVT analysis and Process corners, RC delay, Elmore Delay, Logical Effort, Electrical Effort, Parasitic delay, Non-ideal delay, Examples **07 Hrs**

Unit-IV

Combinational MOS Logic Circuits & Sequential MOS Logic Circuits: Introduction, MOS logic circuits with depletion nMOS loads, CMOS logic circuits, complex logic circuits, CMOS Transmission gate, Introduction to sequential MOS logic circuits, Behavior of bi-stable elements, SR latch circuit, clocked latch and flip flop circuits **08 Hrs**

Unit-V

Dynamic Logic Circuits: Introduction, Basic principles of Pass transistor circuits, voltage bootstrapping, synchronous dynamic circuit techniques, dynamic CMOS circuit techniques, high performance dynamic CMOS circuits **08 Hrs**

Reference Books:

1) Sung Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3/e, McGraw-Hill, 2008.
2) Kanaan Kano, “Semiconductor Devices”, 3/e,Pearson education, 2004.
3) Douglas A Pucknell & Kamran Eshragian, “Basic VLSI Design”, 3/e, PHI, 2005.
4) Michael John Sebastian Smith “Application Specific Integrated Circuits”, Pearson Publication, 2013.

21UECC501	Microwave and Antennas	(2-2-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs): The course focuses on the study of microwave propagation through waveguide tubes, and properties of various types of microwave components. It deals with the working principle of various microwave sources and their applications. The course also deals with the basics of antenna theory, construction, design, working principle, radiation pattern and applications of various types of antennas. It also deals with radio waves propagation.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the modes of microwave propagation in a rectangular waveguide tube	1,2	3	
CO-2	**Derive** the scattering matrix for waveguide components and **understand** the working principle of microwave sources	1,2	3	
CO-3	**Understand** the terminologies of antennas			1,12
CO-4	**Derive** the radiation pattern of array of point sources, dipole, thin linear antennas and **analyze** their characteristics	1,2,3		13
CO-5	**Design** of various antenna types and understand radio wave propagation	1,2,3		13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.6	3.0	2.0	-	-	-	-	-	-	-	-	1.0	1.0	-

Pre-requisites: Engineering Physics

Contents:

Unit-I

Review of Electromagnetics: Maxwell's equations, wave equations.

Introduction to Microwaves: Microwave frequency bands, applications of microwaves.

Rectangular waveguides: Propagation of waves in a rectangular waveguide, modes, TE and TM modes, propagation of TE and TM modes in rectangular waveguides. **08 Hrs**

Unit-II

Waveguide Components: Waveguide Tees (T-Junctions), directional coupler, circulator and isolator**.**

Microwave Tubes: Two cavity Klystron amplifier, Reflex Klystron oscillator, applegate diagram, construction and working principle of magnetron and travelling wave tube.

Transferred electron and avalanche transit time devices: Gunn-effect diode, modes of operation, IMPATT Diode, TRAPATT Diode. **07 Hrs**

Unit-III

Antenna Basics: Introduction, Basic Antenna parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Directivity & Resolution, Antenna apertures, Effective height, Radio Communication link, Fields from oscillating dipole, Antenna Field Zones, Linear, Elliptical & Circular polarization. **07 Hrs**

Unit-IV

Point Sources and Their Arrays: Introduction, Point Source defined, Power patterns, Power theorem, Radiation intensity, Examples of Power patterns, Field patterns, Phase patterns, Arrays of two Isotropic Point sources, Non-Isotropic but similar Point Sources and Principle of pattern multiplication, Non-isotropic and Dissimilar Point sources, Linear Arrays of n Isotropic Point sources of equal amplitude and spacing.

Electric Dipoles and Thin Linear Antennas: Introduction, Short electric dipole, Fields of a short dipole, Radiation resistance of short dipole, Radiation resistance of $\lambda/2$ antenna. **08 Hrs**

Unit-V

Antenna Types: Introduction, Small loop, Comparison of far fields of small loop and short dipole, Loop antenna general case, Far field patterns of Circular Loop, Radiation resistance of loops, Helical Antennas, Parabolic Reflectors, Log Periodic Antenna.

Radio Wave Propagation: Introduction, Ground wave propagation, Free Space propagation, Ground reflection, Surface wave, Diffraction, Tropospheric propagation: Tropospheric scatter, Ionospheric propagation, Structure of the

Ionosphere, Electrical properties of the Ionosphere, Effects of earth's magnetic field, Propagation characteristics of Radio waves for different frequencies, Simple definitions. **09 Hrs**

Reference Books:

1) W H Hayt, J A Buck, "Engineering Electromagnetics", Tata McGraw-Hill publications, 2007
2) M. Kulkarni, "Microwave and Radar Engineering", Umesh publications, 2003.
3) Samuel Y. Liao, "Microwave Devices and Circuits", 4th Edition, Pearson, 2008.
4) D. Kraus, Ronald J. Marhefka, Ahmad S. Khan "Antennas for all Applications", 4/e, McGraw-Hill edition, 2010.
5) K. D. Prasad "Antenna & Wave Propagation", Satya Prakashana, New Delhi, 1999.

21UECC502 Object Oriented Programming using C++ (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course is aimed at the basics of object-oriented programming. The language selected for illustrating the concepts is C++. The course deals with functions and discusses the classes and objects. Then inheritance concepts are introduced. This is followed by polymorphism and templates. Real life examples help in understanding the significance of the course.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Apply** the concepts of subroutines to a given real-life problem.	-	1,2,13	3, 5
CO-2	**Understand and Apply** the concepts of classes and objects.	-	1,2,3	12
CO-3	**Develop** the solutions using operator overloading and inheritance.	-	1,2,3	12
CO-4	**Write** the object-oriented code using pointers and virtual functions.	-	1,2,3	12,5
CO-5	**Understand** and **implement** the operational aspects of polymorphism and templates.	-	1,2,3	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.0	-	1.0	-	2.0	-	-	3.0	-	-	-	1.0	-	-

Pre-requisites: Basic programming concepts.

Contents:

Unit-I

Introduction to C++: Programming basics, structures, example programs.
Functions: Simple Functions, Passing Arguments to Functions, Returning Values from Functions, Reference Arguments, Overloaded Functions, Recursion, Inline Functions. **07 Hrs**

Unit-II

Classes and Objects : A Simple Class, C++ Objects as Physical Objects, C++ Objects as Data Types, Constructors, Destructors, Objects as Function Arguments, The Default Copy Constructor, Returning Objects from Functions, A Card-Game Example, Structures and Classes, Classes, Objects, and Memory. **08 Hrs**

Unit-III

Operator Overloading and Type Conversions: Overloading Unary Operators, Overloading Binary Operators, Data Conversion, Operator Overloading Examples.
Inheritance: Derived Class and Base Class, Derived Class Constructors, Overriding Member Functions, example programs, Class Hierarchies, Public and Private Inheritance, Levels of Inheritance, Multiple Inheritance, Ambiguity in Multiple Inheritance, **08 Hrs**

Unit-IV

Pointers, Virtual Functions: Addresses and Pointers, The Address-of Operator, Memory Management: new and delete, Pointers to Objects, basics of Virtual Functions, Friend Functions, the 'this' Pointer, programming examples. **08 Hrs**

Unit-V

Polymorphism: Compile-time polymorphism, run-time polymorphism.
Templates: Introduction, Function Templates, Class Templates, programming examples. **08 Hrs**

Reference Books:

1) Robert Lafore, "Object Oriented Programming using C++", Galgotia Publications, fourth edition, 2004.

2) Herbert Schildt, “C++: The Complete Reference”, fourth edition, McGraw Hill OSBORNE publications.
3) K R Venugopal, Rajkumar, T Ravishankar, “Mastering C++”, Second Edition, Tata McGraw Hill Publishing Company Limited, New-Delhi.
4) S. B. Lippman& J. Lajoie, “C++ Primer”, third edition, Addison Wesley, 2000.

21UECE551	Operating system	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on basic components of a computer operating system, and the interactions among the various components. The course will cover an introduction on the policies for scheduling, deadlocks, memory management, synchronization, system calls, and file systems.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Explain the services, system calls, process, inter process communication and should be able to solve process scheduling problems	3	1,2	-
CO-2	Understand the process synchronization, critical section, deadlock and solve related problems.	-	1,2,3	14
CO-3	Illustrate various ways of main memory organization, techniques of Memory allocation and Paging.	-	3,12	-
CO-4	Elaborate the demand paging, File accessing methods, directory structure and solve page replacement problems.	-	3,14	-
CO-5	Summarize the disk allocation, scheduling and space management.	-	2	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2	2	2.25	-	-	-	-	-	-	-	-	2	**-**	**1.45**

Pre-requisites: Computer organization, Programming fundamentals.

Contents:

Unit-I

Process Scheduling: Introduction to Operating System (OS), OS Services, System calls, Process concept, Process scheduling, Operation on processes, cooperating processes, Inter process communication. CPU scheduling- Basic concepts, scheduling criteria, scheduling algorithms. **08 Hrs**

Unit-II

Process issues: The Critical section problem, Synchronization hardware, Semaphores, problems of synchronization, Critical regions. Deadlock - System model, Deadlock characterization, Methods for handling deadlocks - Deadlock prevention, deadlock avoidance, Deadlock detection and solution for deadlock. **09 Hrs**

Unit-III

Main Memory Management: Overview, Main memory management- Background, Swapping, Contiguous allocation, Paging, Segmentation, Segmentation with paging. **07 Hrs**

Unit-IV

Virtual memory: Background, Demand paging, Process creation, Page replacement algorithms, Allocation of frames, thrashing. File System interface - File concept, Access methods, Directory structure, File system mounting, File system implementation. **08 Hrs**

Unit-V

Secondary Memory Management: Directory implementation, Allocation methods and free space management. Mass storage structures – Disk structure, Disk scheduling methods, Disk management, Swap space management. **07 Hrs**

Reference Books:

1) Abraham Silberschatz, Peter Baer Galvin, Greg Gagne ─ “Operating System Concepts”, 6thedition, John Wiley & Sons.
2) Milan Milankovic, “Operating system concepts and design”, 2ndEdition, McGraw- Hill.
3) Harvey M. Deital , “Operating systems”, Addison Wesley Publications.
4) D.M Dhamdhere, “Operating systems - A concept based Approach”, Tata McGraw-Hill the Operating systems.

21UECE552	IoT and Applications	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses about the fundamentals of Internet of Things and its building blocks along with their characteristics and gain insights about the current trends of Associated IOT technologies and IOT Analytics

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Describe the evolution of IoT, IoT networking components, and addressing strategies in IoT	-	2	1
CO-2	Classify various sensing devices and actuator types.	-	1,2	-
CO-3	Demonstrate the processing in IoT.	3	2,12	-
CO-4	Explain Associated IOT Technologies	5	3,13	1,2
CO-5	Illustrate architecture of IOT Applications	5	2,12	14

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.33	1.8	2.5	-	3	-	-	-	-	-	-	2	2	1

Pre-requisites: Basics of Computer

Contents:

Unit-I

Basics of Networking: Introduction, Network Types, Layered network models Emergence of IoT: Introduction, Evolution of IoT, Enabling IoT and the Complex Interdependence of Technologies, IoT Networking Component **08 Hrs**

Unit-II

IoT Sensing and Actuation: Introduction, Sensors, Sensor Characteristics, Sensorial Deviations, Sensing Types, Sensing Considerations, Actuators, Actuator Types, Actuator Characteristics. **08 Hrs**

Unit-III

IoT Processing Topologies and Types: Data Format, Importance of Processing in IoT, Processing Topologies, IoT Device Design and Selection Considerations, Processing Offloading. **08 Hrs**

Unit-IV

Associated IoT Technologies Cloud Computing: Introduction, Virtualization, Cloud Models, Service-Level Agreement in Cloud Computing, Cloud Implementation, Sensor-Cloud: Sensors-as-a-Service. IoT case studies, Agricultural IoT – Introduction and Case Studies **08 Hrs**

Unit-V

IoT Case Studies and Future Trends: Vehicular IoT – Introduction Healthcare IoT – Introduction, Case Studies IoT Analytics – Introduction **07 Hrs**

Reference Books:

1) Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)",1st Edition, VPT, 2014.

2) S. Misra, C. Roy, and A. Mukherjee, 2020. Introduction to Industrial Internet of Things and Industry 4.0. CRCPress.

3) Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.

21UECE553 Automotive Electronics (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on Electronic Engine control system, construction and operation of sensors and actuators, role of electronics in vehicle motion control, instrumentation and advanced features for safety and comfort in vehicles.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyse** and **examine** the Engine control system with respect to various performance terms	-	1	-

CO-2	**Analyse** and **apply** various Sensors and Actuators in the Engine control applications.	3	7	2
CO-3	**Describe** and **design** various digital subsystems for power train control.	-	5	13
CO-4	**Analyse** and **design** various subsystems of Vehicle Motion Control and Occupant Protection System.	-	2	14
CO-5	**Analyse** and **design** various subsystems of Automotive Instrumentation and Telematics.	6	4	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.0	1.5	3.0	2.0	2.0	3.0	2.0	-	-	-	-	1.0	1.0	1.0

Pre-requisites: Basics of Automobiles and Engines, Analog and Digital Electronic Circuits, Control systems and microcontrollers.

Contents:

Unit-I

The Basics of Electronic Engine Control: Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Federal Government Test Procedures, Concept of an Electronic Engine Control System, Definition of Engine Performance Terms, Exhaust Catalytic Converters, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition. **08 Hrs**

Unit-II

Sensors and Actuators: Control system applications of sensors and actuators, Throttle Angle Sensor, Temperature Sensors, Typical Coolant Sensor, Sensors for Feedback Control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Stepper Motors, Ignition System. **08 Hrs**

Unit-III

Digital Powertrain Control Systems: Introduction, Digital Engine Control, Digital Engine Control Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System. **08 Hrs**

Unit-IV

Vehicle-Motion Controls and Occupant Protection Systems: Representative Cruise Control System, Cruise Control Electronics, Antilock Braking System,

Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering, Occupant Protection Systems **07 Hrs**

Unit-V

Automotive Instrumentation and Telematics: Modern Automotive Instrumentation, Input and Output Signal Conversion, Advantages of Computer-Based Instrumentation, Display Devices, LED, LCD, VFD, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High-Speed Digital Communications (CAN), Trip Information Computer, Telematics, GPS Navigation, The GPS System Structure, Automotive Diagnostics **08 Hrs**

Reference Books:

1) William B. Ribbens, "Understanding Automotive Electronics", 7/e, Elsevier,2012.
2) A. K. Babu, " Automotive Electrical and Electronics", 2/e, Khanna publishing,2016
3) Tom Denton, "Automobile Electrical and Electronic Systems", 5/e, Institute off Motor Industry, 2017
4) Najamuz Zaman, "Automotive Electronics Design Fundamental'' first edition, Springer 2015.

21UECL504 Communication Systems Laboratory (0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The course focuses on experiments highlighting the design and demonstration of filters, tuned amplifiers, generation and detection of various analog, pulse and digital modulation techniques. It also includes experiments related to microwave communication.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Moderate Level (2)	**Moderate Level (2)**	**Moderate Level (2)**
CO-1	**Design** and plot the frequency response of active filters and class C tuned amplifier	1,3	2,13	9,12
CO-2	**Generation** and **detection** of various amplitude modulation techniques	1,3	13	9,12

CO-3	**Generation** and **detection** of various pulse modulation techniques	1,3	13	9,12
CO-4	**Generation** and **detection** of various digital modulation techniques	1,3	13	9,12
CO-5	**Demonstrate** the characteristics of microwave sources and devices	**-**	1,13	9,12

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2.8	2.0	3.0	-	-	-	-	-	1	-	-	1.0	1.0	-

List of Experiments:

(1) Design of Band pass filter and Notch filter
(2) Design tuned amplifier, find centre frequency, bandwidth and quality factor
(3) Amplitude modulation using transistor/FET and detection using envelop detector
(4) DSBSC generation using Ring Modulator
(5) Verification of sampling theorem using flat top sampling and reconstruction
(6) Pulse Amplitude Modulation and demodulation
(7) Pulse Width Modulation
(8) ASK modulation and demodulation
(9) FSK, PSK modulation
(10) Measurement of guide wavelength and frequency

Reference Books:

1) Simon Haykin, “An introduction to analog and digital communications”, John Wiley India Pvt. Ltd., 2008.
2) Simon Haykin, “Digital Communications”, John Wiley India Pvt. Ltd., 2009.
3) Samuel Y. Liao, “Microwave Devices and Circuits”, 4thEdition., Pearson, 2008.
4) M. Kulkarni, “Microwave and Radar Engineering”, Umesh Publications, 3rd edition, 1998.

21UECL505 Object Oriented Programming using C++ Laboratory (0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The laboratory is aimed at introducing the students to the basic object-oriented programming. The various features of the object-oriented paradigm are explored using sample programs taken from the real-life situations. The laboratory deals with programs which use various C++ user-defined methods and data members.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Apply** the concepts of recursive subroutines and modular programming to a given problem.	-	1,2	3, 5
CO-2	**Develop** the constructor/ destructor and member functions for a class.	-	1,2,3	5, 12
CO-3	**Develop** the code using operator overloading and inheritance concepts.	-	1,2,3	5, 12
CO-4	**Write** the object-oriented code using pointers and dynamic memory management operators.	-	1,2,3	5, 12
CO-5	**Implement** the class template for a given functionality.	-	1,2,3	5, 12

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2.0	2.0	1.8	-	1.0	-	-	-	-	-	-	1.0	**-**	**-**

Pre-requisites: Basic programming concepts.

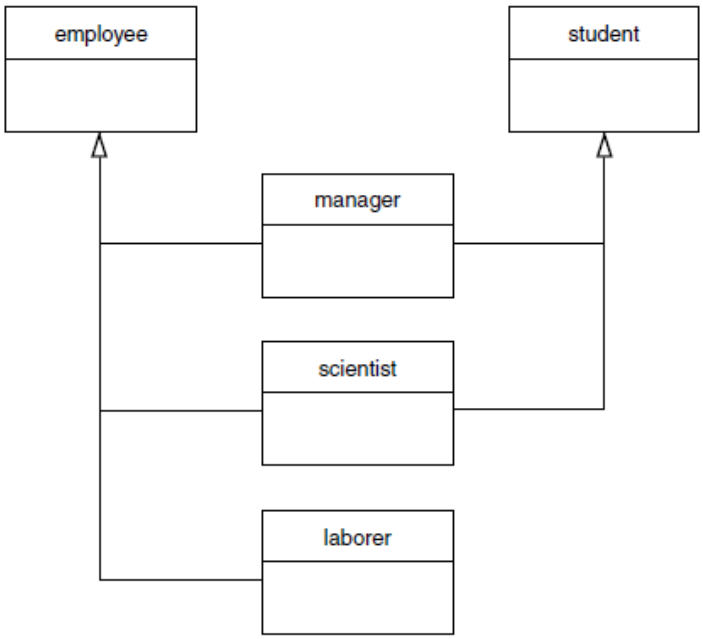
List of Experiments:

1) Write separate recursive functions to find
   a. the first ‘n’ Fibonacci numbers.
   b. the factorial of a given number.

   Read the value of ‘n’ from the user. Perform any possible error checking. Display the output on the screen.
2) Develop a C++ model for implementing a card game. The program needs to imitate a game played by cardsharps (professional gamblers) at carnivals. The cardsharp shows you three cards, then places them face down on the table and interchanges their positions several times. If you can guess correctly where a particular card is, you win. Everything is in plain sight, yet the cardsharp switches the cards so rapidly and confusingly that the player almost always loses track of the card and loses the game.

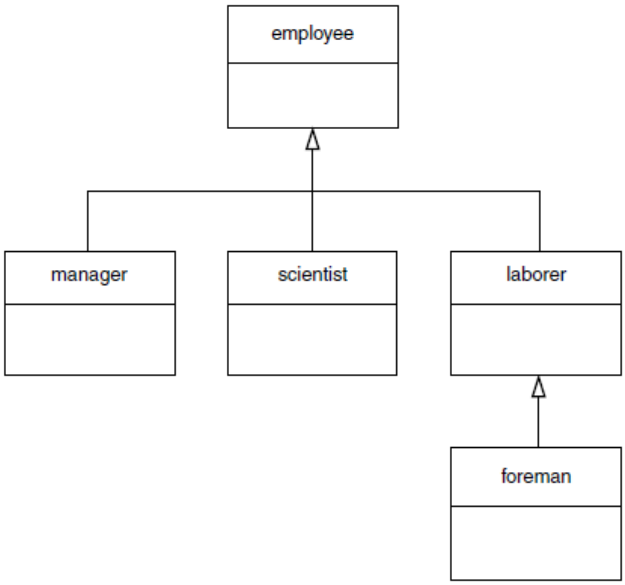
3) Write a C++ program to read the English Distance values expressed in feet and inches. Read two sets of values and perform the addition of those two values. Write the appropriate constructor and destructor functions, member functions. Display the result on the screen.
4) A company has MAX number of employees. Each employee is characterized by the name, employee ID, experience (in years), department, salary (in Rupees). Write a menu-driven code for implementing the following operations.
    a. Display the data of an employee for a given ID.
    b. Display all those employee names with experience greater than a given value.
    c. Display the employees of a certain given department.

    Write the appropriate constructor and destructor functions. Write separate member functions for the above operations.
5) Write an overloaded C++ program to increment the value of an English Distance measured in feet and inches. Write separate functions for pre-increment and post-increment operations. Write the appropriate constructor and destructor functions. Write separate member functions to read the data, and display the results on the screen.
6) Write a C++ program for modelling an instance of multiple inheritance as shown below.



The employee class stores the employee's name and number (ID). student class stores the name of the school or university last attended and the highest degree received. The manager class stores the title and the golf club dues. The scientist class stores the count of publications. Write the various member functions for reading and writing the data.

7) Develop a C++ model for implementing various levels of inheritance as shown below. Assume the functionalities as in Q. No. 6. Write the various member functions for reading and writing the data. Check the order of execution of constructor functions.



8) Develop a C++ model to perform inventory control of a certain automobile manufacturing plant. The class 'part' has data members like name of component, weight, length, width, height, cost, number of units in stock. Write a menu-driven code
   a. to include a new component
   b. to display the data of all the components.
   c. to display all those components which are out of stock.
   d. to delete all the data of components when exiting the program.

   Use dynamic memory management techniques including 'new' and 'delete' operators. Write the appropriate constructor and destructor functions.
9) Develop a C++ model for convolving two discrete-time sequences x1[n] and x2[n]. The input can be of type integer or float. Write the appropriate constructor and destructor functions. Also write separate member functions for reading the sequences, calculating the convolution, and displaying the output. For output display, use overloaded functions.
10) Implement a C++ class template to implement stack operations, namely push and pop. Assume the size of stack as MAX. Perform any possible error checking.

Reference Books:

1) Robert Lafore, "Object Oriented Programming using C++", Galgotia Publications, fourth edition, 2004.
2) Herbert Schildt, "C++: The Complete Reference", fourth edition, McGraw Hill OSBORNE publications.

3) K R Venugopal, Rajkumar, T Ravishankar, “Mastering C++”, Second Edition, Tata McGraw Hill Publishing Company Limited, New-Delhi.
4) S. B. Lippman & J. Lajoie, “C++ Primer”, third edition, Addison Wesley, 2000.

21UAEE550	System Verilog	(2-0-0) 2

Contact Hours: 26

Course Learning Objectives (CLOs):

The course focuses on coding guidelines for system Verilog, data types, data structures supported, structures and unions, and subroutines.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1-12)/ PSOs (13,14)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Establish** the relevance of System Verilog as a (Hardware Description and Verification Language) HDVL.	-	1	-
CO-2	**Understand** the importance and Guidelines of System Verilog	-	1	-
CO-3	**Identify** the Language constructs and their usage.	-	1,2,3	4
CO-4	**Emphasize** on the importance of utilization of Data structures (array, structure and unions).	-	1,2,3	4,13,14
CO-5	**Demonstrate** the importance of subroutines and utilize it to provide better solutions	-	1,2,3	4,13,14

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2	2	2	1	-	-	-	-	-	-	-	-	1	1

Pre-requisites: Verilog, Programming using C++ and Digital System Design.

Course Contents:

UNIT I

Introduction to System Verilog-I: System Verilog origins, Generations of the System Verilog standard, Donations to System Verilog, Key System Verilog enhancements for hardware, design, System Verilog Declaration Spaces,

Packages, Package definitions, Referencing package contents, Synthesis guidelines, $unit compilation-unit declarations. **05 Hrs**

UNIT II

Introduction to System Verilog-II: Coding guidelines, System Verilog identifier search rules, Source code order, Coding guidelines for importing packages into $unit, Synthesis guidelines, Declarations in unnamed statement blocks, Local variables in unnamed blocks, Simulation time units and precision, Verilog's timescale directive, Time values with time units, Scope-level time unit and precision, Compilation-unit time units and precision. **05 Hrs**

UNIT III

System Verilog Literal Values and Built-in Data Types: Enhanced literal value assignments 'define enhancements, System Verilog variables, using 2-state types in RTL models,2-state type characteristics, Relaxation of type rules, Signed and unsigned modifiers, Static and automatic variables, Deterministic variable initialization, Type casting, Constants System Verilog User-Defined and Enumerated Types, User-defined types, Enumerated types. **06 Hrs**

UNIT IV

System Verilog Arrays, Structures and Unions: Structures. Unions, Arrays, The for each array looping construct X, Array querying system functions, The $bits "sizeof" system function, Dynamic arrays, associative arrays, sparse arrays, and strings. **05 Hrs**

UNIT V

System Verilog Procedural Blocks, Tasks and Functions: Verilog general purpose always procedural block, System Verilog specialized procedural blocks, Enhancements to tasks and functions. **05 Hrs**

Reference Books:

1) Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design A Guide to Using System Verilog for Hardware Design and Modeling", Second Edition, Springer Publications, 2006
2) Chris Spear and Greg Tumbush "System Verilog for Verification A Guide to Learning the Testbench Language Features", Third edition, Springer Publications, 2012
3) Mark Zwolinski "Digital System Design with System Verilog", Pearson Education, 2009
4) Mike Mintz, Robert Ekendahl, "Hardware Verification with System Verilog: An Object-Oriented Framework", Springer Publications, 2007.
5)

21UAEE551	Python Programming	(2-0-0) 2

Contact Hours: 26

Course Learning Objectives (CLOs):

This course focuses on concepts of Python programming. It discusses the various fundamental building blocks of Python program. Various data structures like lists, tuples, dictionaries and files are covered in this subject. This is followed by an introduction to various file handling operations and debugging concepts.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** proficiency in handling loops and creation of functions.	-	5	1,3
CO-2	**Identify** the methods to create and manipulate lists, tuples and dictionaries.	-	5	-
CO-3	**Develop** programs for string processing and file organization	-	5	-
CO-4	**Interpret** the concepts of file-related operations in Python.	-	5	-
CO-5	**Debug** the Python programs and able to perform operations on folders.	-	5	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.0	-	1.0	-	2.0	-	-	3.0	-	-	-	1.0	-	-

Pre-requisites: Basic programming concepts.

Contents:

Unit-I

Python Basics: Entering Expressions into the Interactive Shell, The Integer, Floating-Point, and String Data Types, String Concatenation and Replication, Storing Values in Variables, Your First Program, Dissecting Your Program.

Flow control: Boolean Values, Comparison Operators, Boolean Operators, Mixing Boolean and Comparison Operators, Elements of Flow Control, Program Execution, Flow Control Statements, Importing Modules, Ending a Program Early with sys.exit(). **06 Hrs**

Unit-II

Functions: def Statements with Parameters, Return Values and return Statements, The None Value, Keyword Arguments and print(), Local and Global Scope, The global Statement, Exception Handling, A Short Program: Guess the Number.

Lists: The List Data Type, Working with Lists, Augmented Assignment Operators, Methods, Example Program: Magic 8 Ball with a List, List-like Types: Strings and Tuples, References. **05 Hrs**

Unit-III

Dictionaries and Structuring Data: The Dictionary Data Type, Pretty Printing, Using Data Structures to Model Real-World Things.

Manipulating Strings: Working with Strings, Useful String Methods, Project: Password Locker, Project: Adding Bullets to Wiki Markup. **05 Hrs**

Unit-IV

Reading and Writing Files: Files and File Paths, The os.path Module, The File Reading/Writing Process, Saving Variables with the shelve Module, Saving Variables with the print.format() Function. **05 Hrs**

Unit-V

Organizing Files: The shutil Module, Walking a Directory Tree, Compressing Files with the zipfile Module, Renaming Files with American-Style Dates to European-Style Dates, Backing Up a Folder into a ZIP File.

Debugging: Raising Exceptions, Getting the Traceback as a String, Assertions, Logging, IDLE‟s Debugger. **05 Hrs**

Reference Books:

1) Al Sweigart,“Automate the Boring Stuff with Python”,1st Edition, No Starch Press, 2015.
2) Allen B. Downey, “Think Python: How to Think Like a Computer Scientist”, 2nd Edition,Green Tea Press, 2015.
3) Christian Hill, “Learning Scientific Programming with Python”, Cambridge University Press, 2015.
4) Sandeep Nagar, “Introduction to Python for Engineers and Scientists: Open Source Solutions for Numerical Computation”, Apress Publication, 2018.

21UECL506	Minor Project-I	(0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

Minor project-I is introduced at V semester level to encourage students mainly to solve real time societal problems by integrating the knowledge gained in previous semesters. It may involve the investigation of a problem and the specification and implementation of a solution. Minor project-I helps the students to develop problem solving, analysis, synthesis and evaluation skills. It also helps in developing collaborative work culture and team work. In focus with this, students understand the basics of electronics, communication and programming languages in depth and then work on planning, analyzing, designing and executing a hardware/software project.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** technical / social problem and **formulate** a problem statement	1,2	6	-
CO-2	**Propose** technical approach towards solution	2	6,7	11
CO-3	**Implement** the solution in hardware and / or software	3,5	13,14	11
CO-4	**Organize** the topics in a systematic manner and **Prepare** the report in a specific format	9,10	12	-
CO-5	**Present** the work in a systematic manner	10	12	-

POs/PSO	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	3	3	3	-	3	2	2	-	3	3	1	2	2	2

Prerequisites:

Basics of Electronics, Communication and Programming languages

Guidelines for Conduction Spirit of the Course:

To ensure that undergraduates successfully apply the knowledge they have gained in different courses and integrate material learnt at different stages of the curriculum up to the 5th semester so as to complete the project work within the stipulated time duration following guidelines are framed.

1. Project groups are formed with 3-4 students in each team.
2. Project coordinators instruct student project batches to submit synopsis in the prescribed format in the field of their choice.
3. Project coordinators allot guides based on their field of specialization. However students can have further discussions on the project topic and can modify their project title.
4. Students are instructed to report to their respective guides on weekly basis for discussion.
5. Students are instructed to maintain separate project diary/notebook to show the progress work while having discussion with guide and review committee members.
6. Two reviews are fixed in a semester to monitor the progress of the project.

Assessment: CIE- Guides evaluate project for 30 marks and 20 marks are allotted by reviewers by conducting 2 reviews. Total marks for project is 50 (CIE only). **SEE:** There is no semester end exam (SEE) component for Minor project-I.

Note:

- Designated committee is constituted with 2-4 committee members to monitor the process of Mini Project-I
- An internal guide is allotted per group who guides and monitors the project progress.
- Problem statements can be derived from industry, society, etc., after interacting with them.
- Course outcomes (4 or more) are written and mapped to program outcomes and program specific outcomes. In addition to that other POs can also be included if those POs are deemed suitable.
- At the end of the course, students are required to document the project in the form of report.

21UECL507	Internship-I	2 Weeks

Course Learning Objectives (CLOs):

The students have to undergo internship in Private industries/R&D organizations/ Centres of Excellence/Laboratories of Reputed Institutions/Govt. & Semi Govt. organizations, PSUs, construction companies, entrepreneurial organizations, inter departments within the college etc. to get an exposure to the external world for a period of 2 weeks in the summer vacation after IV semester and before start of V semester. The students must prepare a report on the internship work carried out. The internal faculty shall monitor the students and award CIE marks.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Acquire** practical experience in an organizational setting	1,2	-	-
CO-2	**Apply** the knowledge and skill set in engineering design processes appropriate to the internship program.	1,2,3,4	5	-
CO-3	**Apply** modern tools and processes to solve the live problems.	5	3,4	-
CO-4	**Get** an opportunity to learn new skills	10	11	-
CO-5	**Learn** strategies like time management, multi-tasking, communication and team work skills in an industrial setup.	8,9	12	-

POs/PSO	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	**3**	**3**	**2.5**	**2.5**	**2.5**	**-**	**-**	**3**	**3**	**3**	**2**	**2**	**-**	**-**

VI Semester

21UECC600	Analog and Mixed Mode VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the basic requirements of circuit design, difficulties in the design phase and various circuit examples. The course considers widely used analog circuits such as OPAMP, ADC, DAC, current source and sinks, mirrors and PLL as examples for the discussion.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the characteristics and short channel effects of MOS devices	-	-	1
CO-2	**Analyze and design** various configurations (CS, CD, CG) of single stage amplifiers.	2,3,13	-	1
CO-3	**Design** the analog circuits such as op-amps, current sources, current sinks and current mirrors.	2,3,13	-	-
CO-4	**Compare** data converter characteristics and **build** data converter architectures.	13,14	4,5	-
CO-5	**Explain** PLL and its applications.	1,13	-	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.66	3	3	2	2	-	-	-	-	-	-	-	3	3

Pre-requisites: Analog Electronics, Network Analysis, Digital circuits & Basics of CMOS VLSI Design.

Contents:

Unit-I

Introduction to Analog Design: Introduction to MOS, MOS V/I characteristics, second order effects, MOS device models.

Common source single stage amplifiers: Basic concepts, common source stage with resistive load, diode connected load, current source load, triode load and source degeneration. **10 Hrs**

Unit-II

Other single stage amplifiers: source follower, Common gate stage, Cascode stage.

Current Sinks, Current Sources and Current Mirrors: Current sinks and sources, techniques to improve performance of current sinks and sources, current mirrors, effects to cause current mirror to be different from ideal situation.

08 Hrs

Unit-III

Operational Amplifiers: General considerations, Single stage Op-Amps, two stage Op-Amps, gain boosting, comparison, common mode feedback, slew rate, power supply rejection ratio, Comparator.

06 Hrs

Unit-IV

Data Converter fundamentals and architectures: Introduction, sample and hold characteristics, digital to analog converter (DAC) specifications, analog to digital converter (ADC) specifications, DAC architectures: Resistor string, R-2R ladder network, Charge scaling DACs, ADC architectures: Pipeline ADC, Successive approximation ADC. **09 Hrs**

Unit-V

Phase Locked Loops: Simple PLL, Basic PLL Topology, Dynamics of Simple PLL, Charge Pump PLLs, Non ideal effects in PLLs, Delay Locked Loops and Applications. **06 Hrs**

Reference Books:

1) Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill Edition 2008.
2) R. Jacob Baker, Harry W. LI, David E. Boyce, “CMOS Circuit Design, lay out and Synthesis”, IEEE press, 2005.
3) Phillip E. Allen, Douglas R. Holberg, “CMOS Analog Circuit Design”, 2/e, New York Oxford, Oxford University.
4) Adel S. Sedra, Kenneth C. Smith, “Microelectronic Circuits Theory and Applications”, 5th edition Oxford University Press, 2013.

21UECC601	Embedded Systems	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on embedded system concepts, design and its challenges. Design of single embedded processor. Develop the prototype using hardware software co-design approach.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** the architectural features and design issues in ESD	-	2	1
CO-2	Design of single embedded processor	-	1,2	-
CO-3	**Develop** an embedded system application using component engineering.	3	2,12	-
CO-4	**Develop** the hardware software co-design and firmware design approaches.	5	3,13	1,2
CO-5	**Demonstrate** the need of real time operating system	5	2,12	14

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.33	1.8	2.5	-	3	-	-	-	-	-	-	2	2	1

Pre-requisites: Microcontrollers

Contents:

Unit-I

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of embedded systems. Elements of an Embedded System, Differences between RISC and CISC, Harvard and Princeton architectures, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Opt-coupler, Communication Interfaces.

08 Hrs

Unit-II

Embedded system design challenges, common design metrics and optimizing them. Survey of different embedded system design technologies, trade-offs. **Single Purpose Processor:** Introduction, Combinational logic, Sequential logic, Custom single purpose processor design, RT Level custom single purpose processor design and optimizing custom single purpose processors.

08 Hrs

Unit-III

Standard Single Purpose-Peripherals: Introduction, Timers, counters and Watch dog timers, UART, PWM, LCD, Keypad controller and stepper motor controllers, A to D converters. **08 Hrs**

Unit-IV

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling, Embedded firmware design and development **07 Hrs**

Unit-V

Real Time Operating Systems: RTOS basics, Types of operating systems, Task, process and threads, Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores, How to choose an RTOS. **08 Hrs**

Reference Books:

1) Embedded System Design: “A Unified Hardware/Software Approach “Frank Vahid and Tony Givargis,1999
2) Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2nd edition.
3) James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
4) Yifeng Zhu, “Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C”, 2nd E -Man Press LLC ©2015
5) Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003

21UECC602	Computer Communication Networks	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the process of data communication in computer network through the layered architecture. It also deals with the IEEE standards and various protocols at different layers.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** and **Design** the physical layer aspects of Computer Communication Networks.	-	1	-
CO-2	**Analyze** and **Design** the Data link layer aspects of Computer Communication Networks.	1,2	3,14	-
CO-3	**Analyze** and **Design** the physical and Datalink Layer aspects of Wired and Wireless Local Area Networks.	-	1,3	2
CO-4	**Analyze** and **Design** the Network layer aspects of Computer Communication Networks.	2,3	1	-
CO-5	**Analyze** and **Design** the Transport layer aspects of Computer Communication Networks.	-	2,3	4

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.25	2.25	2.25	1.0		-	-	-	-	-	-	-	-	2

Pre-requisites: Analog and Digital Communication

Contents:

Unit-I

Networks: Network Criteria, Physical Structures of Networks, Local Area Network, Wide Area Network, Switching, The Internet, Accessing the Internet, **Network Models:** Principles of Protocol Layering, Logical Connections, Layers in TCP/IP

Protocol Suite and Description of each, Encapsulation and Decapsulation, Addressing, Transmission Media**:** Guided Media, Unguided Media.
Switching: Circuit Switched Networks, Datagram Networks. **08 Hrs**

Unit-II

Data Link Layer: Services, Link-Layer Addressing, Data Link Control (DLC): Framing, Flow and Error Control, Data-link Layer Protocols, Media Access Control: Random Access, Controlled Access, Channelization. **08 Hrs**

Unit-III

Wired LANs - Ethernet: IEEE Project 802, Standard Ethernet, Fast Ethernet, **Wireless LANs:** Architectural Comparison, Characteristics, Access Control, IEEE 802.11 Project, Bluetooth, **Connecting Devices:** Hubs, Link-layer Switches, Routers **08 Hrs**

Unit-IV

Network Layer: Network Layer Services, Packet Switching, IPv4 Address space, Classful Addressing, Classless Addressing, Network Address Translation, Packet forwarding based on Destination Address.
Network Layer Protocols: IPv4 Datagram format, Fragmentation**, Unicast Routing:** Least-Cost Routing, Distance vector Routing, Link-State Routing, Path-Vector Routing **08 Hrs**

Unit-V

Next Generation IP: IPv6 Address Representation, Address Space, Address Space Allocation, IPv6 Packet format, Extension Header.
Transport layer- Transport Layer Services, Connectionless and Connection Oriented Protocols, Go-back N protocol, Selective Repeat Protocol, **Transport Layer Protocols**: UDP User Datagram, UDP Services, TCP Services, TCP Features, TCP Segment **07 Hrs**

Reference Books:

1) Behrouz A. Forouzan, **"Data Communication and Networking"**, 5th Edition, McGraw Hill, 2012.
2) James F. Kurose, Keith W. Ross "**Computer Networks"**, Pearson Education, 3rd Edition, 2007.
3) Wayne Tomasi, **"Introduction to Data communication and Networking"**, Pearson Education, 2007.
4) Andrew S. Tanenbaum, "**Computer Networks**", 5th Edition, Pearson Education, 2013.

21UECE651	Digital Image Processing	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course introduces to the fundamental concepts of image processing. Topics covered include color image processing, various image enhancement techniques, detection of discontinuities, edge linking and boundary detection.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Describe image acquisition system, its representation		1	12
CO-2	Apply suitable image enhancement techniques in spatial and frequency domain	2	1,3	12
CO-3	Compare various restoration techniques	2	1,13	-
CO-4	Conduct independent study in the analysis of color and morphological image processing	2	1,3	12
CO-5	Compare various image segmentation techniques	-	1,13	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2	3	2	-	-	-	-	-	-	-	-	1	2	**-**

Pre-requisites: Digital signal processing

Contents:

Unit-I

Digital Image Fundamentals: Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition. **07 Hrs**

Unit-II

Intensity Transformation: Basic intensity transformation functions, Image negatives, Contrast stretching, Histogram processing, Histogram equalization, Enhancement using arithmetic and Logic operations.

Spatial and Frequency Filtering: Spatial Filter Masks, Smoothing spatial filters, Sharpening spatial filters, Combining spatial enhancement methods, Smoothing frequency domain filters, Sharpening frequency domain filters, Homomorphic filtering. **08 Hrs**

Unit-III

Fundamentals of Image Restoration: Introduction, noise models, Restoration in the presence of noise, Linear position invariant degradation, Degradation function.

Image Restoration Filters: Spatial filtering, Periodic noise reduction by frequency domain filtering, Inverse filtering, Minimum mean square error filtering, Constrained least squares filtering, Geometric mean filter, Geometric transformations. **08 Hrs**

Unit-IV

Color Fundamentals: The physics of color, Human color perception, Representing color, Surface color from image color. color models, pseudo color Image Processing.

Morphological Image Processing: Preliminaries, Erosion and Dilation. **08 Hrs**

Unit-V

Image Segmentation: Detection of discontinuities, Edge linking and boundary detection, Thresholding.

Advanced Topics in Segmentation: Region-based segmentation, Segmentation using morphological watersheds, Use of motion in segmentation. **08 Hrs**

Reference Books:

1) Digital Image Processing-Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010
2) Fundamentals of Digital Image Processing- A K. Jain, Pearson 2004.
3) Image Processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.
4) K.P.Soman, “Digital Signal & Image Processing”, 1/e edition, Elsevier India, 2012

21UECE652	Data Structures using C++	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course deals with the basics of data structures. Linked lists, stack, queues and trees etc. are included. An introductory chapter on pointers helps in the knowledge of data structures. Real life examples enhance the effectiveness of the course.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Apply** various concepts of C++ such as Arrays, Strings, Structures, Unions, Files, Pointers and Functions in solving problems.	-	1,2,13	3
CO-2	**Understand and Implement** the operational aspects of linked lists (using pointers) such as creation, insertion, deletion and searching in problem solving.	-	1,2,3	5, 12
CO-3	**Realize and Implement** the operational aspects of stack in problem solving using Arrays and Pointers.	-	1,2,3	12
CO-4	**Implement** the operational aspects of queue in problem solving using Arrays and Pointers**.**	-	1,2,3	5, 12
CO-5	**Implement** the operational aspects of trees using Arrays and Pointers, and Hash concept in problem solving.	-	1,2,3	5, 12

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2.0	2.0	1.8	-	1.0	-	-	-	-	-	-	1.0	2.0	**-**

Pre-requisites: Object Oriented Programming using C++.

Contents:

Unit-I

Structure, unions and Pointer Revisit: Motivation for using structures. Pointer, access data from memory through pointer, pointer to structures. Motivation for dynamic memory requirement. Realizing arrays using pointer and dynamic memory allocation. Importance of memory management during allocation and de-allocation of memory. **07 Hrs**

Unit-II

Lists: Constructing dynamic data structures using self-referential structure (using the same realized linked Lists), operations on lists. Doubly Linked list. Application of Lists in sorting. **08 Hrs**

Unit-III

Stack: Realization of stack and its operations using static and dynamic structures. Application of stack in converting an expression from infix to postfix and evaluating a postfix expression, Heterogeneous stack using Unions. **08 Hrs**

Unit-IV

Queues: Realization of queues (FIFO, Double-ended queue, Priority queue) and its operations using static and dynamic data structures. **07 Hrs**

Unit-V

Trees: Types of trees and their properties, Realization of trees using static and dynamic data structures. Operations on Binary trees and their application in searching (BST and AVL Tree), Binary heap as priority.

Hash Table: Realizing effective hash table with proper data structure and hash function, its application. **09 Hrs**

Reference Books:

1) Aaron M. Tenenbaum, Yedidyah Langsam and Moche J. Augenstein, “Data Structures using C & C ++”, Pearson Education / PHI, 2006
2) E. Balagurusamy, “Programming in ANSI C”, 4th edition, Tata McGraw Hill, 2008.
3) Behrouz A. Foruzan and Richard F. Gilberg, “Computer Science: A Structured Programming Approach Using C”, 2nd edition, Thomson, 2003.
4) Robert Kruse and Bruce Leung, “Data structures and Program Design in C”, Pearson Education, 2007.

21UECE653	Reconfigurable Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on key criteria: area, speed, optimization techniques employed, various system architectures considered in the FPGA method of Design.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** the basics of FPGA Architecture and its Function mapping.	-	1,2	13,14
CO-2	**Modeling** the languages and its synthesis.	-	1,2	-
CO-3	**Understand** Advanced FPGA design principles w.r.t speed and area.	1,2	-	-
CO-4	**Design** strategies for DSP and Image Processing applications.	3	13,14	5
CO-5	**Analyze** and **explore** the architectural design of FPGA for Deep Learning Applications.	3	13,14	5

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.33	2.33	3	-	1	-	-	-	-	-	-	-	1.66	1.66

Pre-requisites: Knowledge of FPGA and microcontroller architecture

Contents:

Unit-I

FPGA Design Flow: Reconfigurable Logic Devices, Field-Programmable Gate Arrays, Basic Architecture, Example Actel Devices: ACT1 logic module, Shannon's expansion theorem, Routing, Programmable I/O Architectures**,** Specialized Function Blocks: Embedded Microprocessors. Coarse-Grained Reconfigurable Arrays: Raw & PipeRench Architectures. 0**6 Hrs**

Unit-II

Languages and Compilation, Design Cycle, Languages, Algorithmic RC Languages, Hardware Description Languages (HDL): Modelling of Abstraction Level, High Level Compilation, Compiler Phases. Analysis and Optimizations, Scheduling, Low Level Design Flow, Logic Synthesis Technology Mapping, Logic Placement, Signal Routing Configuration Bit streams **08 Hrs**

Unit-III

Architecting Speed & Area Speed: High Throughput, Low Latency, Timing, Add Register Layers, Register Balancing, Reorder Paths. **Area:**Rolling Up the Pipeline, Control-Based Logic Reuse, Resource Sharing, Impact of Reset on Area, Resources Without Reset, Resources Without Asynchronous Reset, Resetting RAM, Utilizing Set/Reset FF Pins. **08 Hrs**

Unit-IV

FPGA Applications: Signal processing applications: Filtering, DSP application building blocks: Efficient Airthmetic, CORDIC, Transforms, Examples: Beam forming, Software Defined Radio. **Image and video processing**: Local Neighbourhood functions, Convolution, Morphological Operations, Feature Extraction & matching. **08 Hrs**

Unit-V

Accelerating the CNN Inference on FPGAs : Introduction, Background on CNNs and Their Computational Workload, General Overview, Inference versus Training, Inference, Layers, and CNN Models, FPGA-Based Deep Learning Computational Transforms: Winograd Transform and Fast Fourier Transform, Loop Unrolling. Loop Tiling. **Approximate Computing of CNN Models**: Approximate Arithmetic for CNNs, Fixed-Point Arithmetic, Dynamic Fixed Point for CNNs. 0**9 Hrs**

Activity Beyond Syllabus: Seminar on Reconfigurable Computing.

Reference Books:

1) M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
2) Steve Kilts,” Advanced FPGA Design Architecture, Implementation, and Optimization”, WILEY INTERSCIENCE, 2007.
3) Mahmoud Hassaballah and Ali Ismail Awad, “Deep Learning inComputer Vision”, CRC Press,Taylor& Francis Group, 2020.
4) Deep Learning by Ian Goodfellow and YoshuaBengio and Aaron Courville, MIT Press.https://www.deeplearningbook.org/

21UECE654	Cloud Computing	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on concepts of Cloud Computing paradigms. It deals with the origin, need and future insights of cloud computing. Fundamentals of Cloud infrastructure, mechanisms, security, quality attributes and pricing, perceptions are targeted by the course.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the concept of Cloud and deployment models.	1,2	6	10,12,14
CO-2	**Describe** and **differentiate** Cloud Architectures.	2,12	4,6	7,9,14
CO-3	**Determine** and **analyze** Cloud Infrastructure and Management Mechanisms..	-	1,2,4	9,10,14
CO-4	**Understand** and **Contrast** Cloud Security Mechanisms	8	6	12
CO-5	**Analyze** Cloud service quality metrics and Cost metrics	8	12,14	11,7

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2.5	2.6	-	2	-	2.0	1.0	3.0	1	1	1.0	1.3	**-**	**1.0**

Pre-requisites:

Knowledge of Computer Architecture, Networking and Security will be appreciated.

Contents:

Unit- I

Understanding Cloud Computing : Origins and Influences, Basic Concepts and Terminology, Goals and Benefits, Risks and Challenges

Fundamental Concepts and Models : Roles and Boundaries, Cloud Characteristics, Cloud Delivery Models**,** Cloud Deployment Models **06 Hrs**

Unit- II

Fundamental Cloud Architectures : Workload Distribution Architecture, Resource Pooling Architecture, Dynamic Scalability Architecture, Elastic Resource Capacity Architecture, Service Load Balancing Architecture, Cloud Bursting Architecture, Elastic Disk Provisioning Architecture, Redundant Storage Architecture

Advanced Cloud Architectures : Hypervisor Clustering Architecture, Load Balanced Virtual Server Instances Architecture, Non-Disruptive Service Relocation Architecture, Zero Downtime Architecture, Cloud Balancing Architecture ,Resource Reservation Architecture, Dynamic Failure Detection and Recovery Architecture Bare-Metal Provisioning Architecture, Rapid Provisioning Architecture, Storage Workload Management Architecture **11 Hrs**

Unit- III

Cloud Infrastructure Mechanisms : Logical Network Perimeter, Virtual Server Cloud Storage Device, Cloud Usage Monitor, Resource Replication, Ready-Made Environment, Container

Cloud Management Mechanisms : Remote Administration System, Resource Management System, SLA Management System, Billing Management System Cloud-based IT resources need to be set **08 Hrs**

Unit-IV

Fundamental Cloud Security : Basic Terms and Concepts, Threat Agents, Cloud Security Threats, Additional Considerations, Flawed Implementations, Security Policy Disparity, Contracts, Risk Management

Cloud Security Mechanisms : Encryption, Hashing, Digital Signature Public Key Infrastructure (PKI), Identity and Access Management (IAM) Single Sign-On (SSO), Cloud-Based Security Groups, Hardened Virtual Server Images **08 Hrs**

Unit-V

Cost Metrics and Pricing Models : Business Cost Metrics, Cloud Usage Cost Metrics, Cost Management Considerations

Service Quality Metrics and SLAs : Service Quality Metrics, Case Study Example,SLA Guidelines **06 Hrs**

Reference Books:

1) Raj Kumar Buyya, James Broberg and Andrzej Goscinski “Cloud Computing Principles and Paradigms” ,2011, Wiley Publication.
2) Thomas Erl, Zaigham Mahmood, and Ricardo Puttini, “Cloud Computing Concepts, Technology & Architecture”, 2nd Edition, 2019, PRENTICE HALL
3) Venkata Josyula, Malcolm Orr and Greg Page “Cloud Computing: Automating the

Virtualized Data Center",2012, CISCO Press.
4) Anthony T. Velte, Toby J. Velte, Ph.D. and Robert Elsenpeter "Cloud Computing: A Practical Approach" ,2011, The McGraw-Hill Companies
5) Ronald L. Krutz, Russell Dean Vines, "Cloud Security A comprehensive Guide to secure Cloud Computing" Wiley.
6) Borko Furht. Armando Escalante, "Handbook of Cloud Computing", Springer

21UECE655 Artificial Intelligence and Machine Learning (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on introduction to the fundamental concepts in artificial Intelligence & machine learning. Topics covered are fundamentals of AI concepts, Knowledge representation, Decision tree learning, Bayesian learning, and instance based learning.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** fundamental understanding of the history of artificial intelligence (AI) and its foundations.	-	2,4	1
CO-2	**Recognize** the characteristics of artificial intelligence systems that make it useful to real-world problems.		2,3	1
CO-3	**Appreciate** the importance of visualization in the data analytics solution.	12	2,4	1,5
CO-4	**Experiment** with a machine learning model for simulation and analysis.	-	2	1
CO-5	**Demonstrate** an ability to share in discussions of AI, its current scope, limitations, and societal implications.	12	4, 5	13

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1	2	2	2	1.5	-	-	-	-	-	-	3	1	-

Pre-requisites: Mathematics

Contents:

Unit-I

Fundamentals of artificial intelligence: What is artificial intelligence? Problems, problem spaces and search, Heuristic search techniques **07 Hrs**

Unit-II

Knowledge representation issues: Knowledge representation issues, Predicate logic, Representation knowledge using rules. Concept Learning: Concept learning task, Concept learning as search, Find-S algorithm, Candidate Elimination Algorithm, Inductive bias of Candidate Elimination Algorithm. **08 Hrs**

Unit-III

Decision Tree Learning: Introduction, Decision tree representation, Appropriate problems, ID3 algorithm. Aritificial Neural Network: Introduction, NN representation, Appropriate problems, Perceptrons, Backpropagation algorithm. **08 Hrs**

Unit-IV

Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting, MDL principle, Bates optimal classifier, Gibbs algorithm, Navie Bayes classifier, BBN, EM Algorithm **08 Hrs**

Unit-V

Instance-Base Learning: Introduction, k-Nearest Neighbour Learning, Locally weighted regression, Radial basis function, Case-Based reasoning. Reinforcement Learning: Introduction, The learning task, Q-Learning **08 Hrs**

Reference Books:

1) Tom M Mitchell,“Machine Lerning”,1 st Edition, McGraw Hill Education, 2017.
2) Elaine Rich, Kevin K and S B Nair, “Artificial Inteligence”, 3 rd Edition, McGraw Hill Education, 2017
3) Simon Rogers, Mark Girolami, “A First Course in Machine Learning”, second edition, CRC Press, 2017.
4) Richard E. Neopolitan & Xia Jiang, “Artificial Intelligence with an introduction to machine learning”, second edition, CRC press 2018.

21UECE656	Information Theory and Coding	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the basic concepts of information theory and different coding techniques such as source coding, channel coding and turbo codes.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** and **evaluate** dependent model and Markoff model of information sources.	-	1,2	3
CO-2	**Construct** the code-words using different source coding algorithms.	3	1,2	5
CO-3	**Design** and **Analyze** linear Block codes and binary cyclic codes for error detection and correction capabilities.	2	3,13	1,5
CO-4	**Analyze** the convolution codes using different techniques.	3	1,2	-
CO-5	**Explain** Concatenated Codes & Turbo Codes.	-	4,5	3

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.75	2.25	2	2	1.5	-	-	-	-	-	-	-	2	-

Pre-requisites: Probability theory, Communication Systems

Contents:

Unit-I

Information Theory : Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources. **08 Hrs**

Unit-II

Source Coding: Basic definitions, Encoding of the source output, Properties of codes, Prefix codes, Kraft McMillan's Inequality, Code efficiency and redundancy,

Shannon's first theorem (Noiseless coding theorem), Shannon-Fano algorithm, Huffman coding. **08 Hrs**

Unit-III

Error Control Coding: Types of errors, types of codes, Linear Block Codes: Matrix description of linear block codes. Error detecting and correcting capabilities of linear block codes, Lookup table decoding using standard array, Single error correcting Hamming codes.

Binary Cyclic Codes: Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation, Error detection and error correction.

09 Hrs

Unit-IV

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, Viterbi Algorithm

07 Hrs

Unit-V

Concatenated Codes & Turbo Codes: Single level Concatenated codes, Multilevel Concatenated codes, Introduction to Turbo coding and their distance properties, Design of Turbo codes. **07 Hrs**

Reference Books:

1) K. Sam Shanmugam, "Digital and analog communication systems", John Wiley, 2005**.**
2) P.S. Satyanarayana. "Concepts of Information Theory & coding", Dynaram Publications, 2005.
3) Daniel J. Costello and Shu Lin, "Error Control Coding: Fundamentals and Applications", Pearson, Second Edition, 2011.
4) Ranjan Bose, "Information Theory, Coding and Cryptography",Tata McGraw-Hill Publication, 2002.

21UECE657	Nano Electronics	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the study of various nanostructures, their properties and applications. The course also focuses on understanding the physical, chemical and fabrication aspects of nanostructures and nanodevices at nanoscale, relevant to the field of electronics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** and **appreciate** the significance of Nanoelectronics, as an emerging area in the field of electronics.	-	1	-
CO-2	**Classify** different microscopic and spectroscopy techniques required to study novel properties of nanostructures.	5	-	-
CO-3	**Identify** various nanostructures, discuss their properties and applications	-	2	3
CO-4	**Discuss** the physical processes occurring in various nanodevices.	-	4	-
CO-5	Understand the applications of nanosensors and photonic nanostructures..	-	13	7

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2	2	1	2	3	-	1	-	-	-	-	-	2	**-**

Pre-requisites: Physics, Electronics, Engineering Mathematics, Material Science

Contents:

Unit-I

Overview of nanoscience and engineering, Development milestones in microfabrication and electronic industry, Moore‘s law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale. Fabrication methods: Top down processes, Bottom up processes, methods describing the growth of nanomaterials, ordering of nanosystems.

08 Hrs

Unit-II

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction

techniques, spectroscopy techniques, Techniques for property measurement: mechanical, electron, magnetic, thermal properties. **07 Hrs**

Unit-III

Inorganic semiconductor nanostructures: Overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **08 Hrs**

Unit-IV

Fabrication techniques: Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, Strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

Physical processes: Modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical, electrical and structural. **08 Hrs**

Unit-V

Nanosensors: Introduction, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Nanobiosensors.

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, MEMS and NEMS. 0**8 Hrs**

Reference Books:

1) Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2) Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology” , John Wiley, Copyright 2006, Reprint 2011.
3) T Pradeep, “Nano: The essentials-Understanding Nanoscience and Nanotechnology”, TMH.
4) Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “ Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

21UECO651	Data Compression	(3-0-0)3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the need for compression and discusses various lossless and lossy compression techniques and their performance measures. It also explains applications of compression algorithms in image, audio, video and text transmission.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** lossy and lossless compression techniques		1	
CO-2	**Understand** the principles of different types of quantization	1,2	3,4	
CO-3	**Explain** various differential encoding methods	1,2	3,4	12,14
CO-4	**Describe** various lossless coding methods.	1,2	3,4	
CO-5	**Understand** various speech, image and video compression standards.		1,2,3,4	12,14

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.6	2.75	2	2	-	-	-	-	-	-	-	1	-	1

Pre-requisites: Digital Signal Processing, Communication Systems, Information Theory and Coding.

Contents:

UNIT I

Introduction: Compression techniques: Lossless Compression, Lossy Compression, measure of performance, modeling & coding.

Mathematical Preliminaries for Lossless and Lossy Compression: Models, Coding, Distortion Criteria: The Human Visual System, Auditory Perception. **08 Hrs**

UNIT II

Scalar Quantization: Introduction, Quantization problem, Uniform Quantizer, Adaptive Quantization: Forward Adaptive Quantization, Backward Adaptive Quantization, Non-uniform Quantization: pdf optimized Quantization, Companded Quantization. **08 Hrs**

UNIT III

Vector Quantization: Introduction, LBG algorithm, Tree structured VQ, Structured VQ, Trellis coded quantization.

Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation, Speech coding, Image coding. **08 Hrs**

UNIT IV

Huffman coding: Huffman Coding Algorithm, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding: Lossless image compression, Text compression, Audio Compression. **07 Hrs**

UNIT V

Arithmetic Coding: Introduction, Coding a sequence: Generating a tag, Deciphering the tag, Generating a binary code, Comparison of Huffman and Arithmetic coding, Adaptive Arithmetic coding, Applications **08 Hrs**

Reference Books:

1) K. Sayood, “Introduction to Data Compression," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.
2) N. Jayant and P. Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video,” Prentice Hall, USA, 1984.
3) D. Salomon, “Data Compression: The Complete Reference”, Springer, 2000.
4) Z. Li and M.S. Drew**,** “Fundamentals of Multimedia,” Pearson Education (Asia) Pvt. Ltd., 2004.

21UECO652	Cryptography	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on study of encryption/ decryption algorithms of different symmetric and asymmetric cryptographic techniques, Hash functions, Message authentication codes & Digital signature algorithms.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** security services, security threats and mechanisms to counter them and **Analyze** different classical encryption and decryption techniques.	2	1,4	-
CO-2	**Analyze** different symmetric cryptographic standards and modular arithmetic concept.	2	1	4
CO-3	**Evaluate** advanced encryption standard (AES).	2	-	4
CO-4	**Apply** the concepts of private and public key encryption techniques to various algorithms.	-	4,14	2
CO-5	**Demonstrate** and **Illustrate** Elliptic curve arithmetic, Hash functions, digital signature algorithms	1	4,14	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.3	2.5	-	1.6	-	-	-	-	-	-	-	-	-	2

Pre-requisites: Communication networks and finite fields.

Contents:

Unit-I

Introduction and Classical Encryption Techniques: Computer Security Concepts, OSI Security Architecture, Attacks, Services and mechanisms, Model for network security, Symmetric cipher model, Substitution techniques, Transposition techniques, Rotor machines, Steganography. **07 Hrs**

Unit-II

Block Cipher and Encryption Standards: S-DES, Block Cipher Principles, DES, Strength of DES, Block cipher design principles, Block cipher modes of operation. **08 Hrs**

Unit-III

Advanced Encryption Standard: Evaluation criteria for AES, AES Structure, AES round functions. AES Key expansion, An AES Example. **07 Hrs**

Unit-IV

Public Key Cryptography and Key Management: Principles of public key cryptosystems, RSA algorithm, Diffie-Hellman key exchange. ElGamal cryptosystem. **08 Hrs**

Unit-V

Elliptic Curve Arithmetic and Hash functions : Elliptic curve arithmetic, Elliptic curve cryptography, Applications of Cryptographic Hash Functions, Secure Hash Algorithm (SHA), Digital Signatures, Digital Signature Standard, **09 Hrs**

Reference Books:

1) William Stallings, “Cryptography and Network Security,” 4/e, Pearson Education (Asia) Pte. Ltd. / Prentice Hall of India, 2011.
2) Behrouz A. Forouzan, “Cryptography and Network Security”, TMH, 3rd Edition, 2015.
3) Atul Kahate, “Cryptography and Network Security”, Tata McGraw-Hill, 2003.
4) Bernard Menezes, “Network Security and Cryptography”, Cengage Learning India Pvt. Ltd, Second Impression 2011.

21UECO653 Electronics in Automobile (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on Electronic Engine control system, construction and operation of sensors and actuators, role of electronics in vehicle motion control, instrumentation and advanced features for safety and comfort in vehicles.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyse** and **examine** the Engine control system with respect to various performance terms	-	1	-
CO-2	**Analyse** and **apply** various Sensors and Actuators in the Engine control applications.	3	7	2

CO-3	**Describe** and **design** various digital subsystems for power train control.	-	5	13
CO-4	**Analyse** and **design** various subsystems of Vehicle Motion Control and Occupant Protection System.	-	2	14
CO-5	**Analyse** and **design** various subsystems of Automotive Instrumentation and Telematics.	6	4	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.0	1.5	3.0	2.0	2.0	3.0	2.0	-	-	-	-	1.0	1.0	1.0

Pre-requisites: Basics of Automobiles and Engines, Analog and Digital Electronic Circuits, Control systems and microcontrollers.

Contents:

Unit-I

The Basics of Electronic Engine Control: Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Federal Government Test Procedures, Concept of an Electronic Engine Control System, Definition of Engine Performance Terms, Exhaust Catalytic Converters, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition. **08 Hrs**

Unit-II

Sensors and Actuators: Control system applications of sensors and actuators, Throttle Angle Sensor, Temperature Sensors, Typical Coolant Sensor, Sensors for Feedback Control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Stepper Motors, Ignition System. **08 Hrs**

Unit-III

Digital Powertrain Control Systems: Introduction, Digital Engine Control, Digital Engine Control Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System. **08 Hrs**

Unit-IV

Vehicle-Motion Controls and Occupant Protection Systems: Representative Cruise Control System, Cruise Control Electronics, Antilock Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering, Occupant Protection Systems **07 Hrs**

Unit-V

Automotive Instrumentation and Telematics: Modern Automotive Instrumentation, Input and Output Signal Conversion, Advantages of Computer-Based Instrumentation, Display Devices, LED, LCD, VFD, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High-Speed Digital Communications (CAN), Trip Information Computer, Telematics, GPS Navigation, The GPS System Structure, Automotive Diagnostics **08 Hrs**

Reference Books:

1) William B. Ribbens, "Understanding Automotive Electronics", 7/e, Elsevier,2012.
2) A. K. Babu, " Automotive Electrical and Electronics", 2/e, Khanna publishing,2016
3) Tom Denton, "Automobile Electrical and Electronic Systems", 5/e, Institute off Motor Industry, 2017
4) Najamuz Zaman, "Automotive Electronics Design Fundamental'' first edition, Springer 2015.

21UECL603	VLSI Laboratory	(0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The course focuses on exploring the theoretical concepts studied as part of subjects, CMOS VLSI Design and Analog and Mixed Mode VLSI Design in practical with the help of Cadence tool framework. The lab introduces the complete custom IC design flow and Analog and Mixed Signal (AMS) flow for Analog circuits, Digital circuits and Analog and mixed signal circuits design respectively.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** the working of digital and analog circuits and **apply** the design steps of VLSI flow to build the schematic and layouts of VLSI circuits.	1, 2	5	13
CO-2	**Design** and **perform** the DC and transient analysis on combinational & sequential VLSI circuits.	2	1,5	-

CO-3	**Design** and **Perform** the DRC, LVS and RC extraction of layout designs of combinational & sequential VLSI circuits.	2	1,5	-
CO-4	**Design** analog and mixed signal circuits **and Evaluate their** performance**.**	3,5	13	-
CO-5	**Compare and evaluate** the performance of VLSI circuits.	2	10,13	1,4,14

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.5	3	3	1	2.25	-	-	-	-	2	-	-	1.6	1

List of Experiments:

Draw the Schematic and Layout for the following digital and analog circuits mentioned below with the help of Cadence tool frame work and verify the following.

a. Schematic: i) DC Analysis ii) Transient Analysis iii) Parametric analysis

b. Layout: i) DRC ii) LVS iii) RCX

1. Design CMOS Inverter with given specifications.
2. Design CMOS two input NAND and NOR gates.
3. Design Transmission gate & Multiplexer using transmission gates.
4. Design XOR, AND & OR gates using transmission gates.
5. Design D F/F, SR F/F sequential circuits.
6. Design 2-bit up-down counter using D F/Fs.
7. Design a Common Source Amplifier with resistive load for given specifications.
8. Design a source follower circuit.
9. Design single stage Differential Amplifier with given specifications.
10. Design single stage OPAMP using common source amplifier with resistive load.
11. Design 4 bit R-2R DAC using Op-amp with given specifications.

Reference Books:

1) Sung Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3/e, McGraw-Hill, 2008.
2) Douglas A Pucknell& Kamran Eshragian, “Basic VLSI Design”, 3/e, PHI, 2005.
3) Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill Edition 2008.
4) R. Jacob Baker, Harry W. LI, David E. Boyce, “CMOS Circuit Design, lay out and Synthesis”, IEEE press, 2005.

21UECL604	Embedded Systems Laboratory	(0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The course focuses on embedded systems design and development. Hardware-software co design process is explored in real-time system design.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Realize** embedded system design using Integrated Development Environment (IDE).	-	1,5	3,7
CO-2	**Develop** simple embedded C applications using RTOS-APIs.	2,5	3	7,12
CO-3	**Construct** embedded systems using sensors and actuators.	2,13,14	4,5	7,9, 12
CO-4	**Execute** basic IoT applications on embedded platform.	1,2,14	4,5,13	9,6
CO-5	**Realize** communication protocols used in embedded systems.	5	13,14	4

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	2.5	3	1.5	1.6	2.4	1	1	-	1	-	-	1	2.3	2.6

List of Experiments:

1. Sample Embedded C-programs.
2. Develop Embedded C-Program for the following interfacing examples
    a. ADC and DAC.
    b. LED and PWM.
    c. Real time clock and serial port.
    d. Keyboard and LCD.
    e. EPROM and interrupt.
3. Demonstrate Inter-Process Communication using Mailbox.
4. Interrupt performance characteristics of ARM Controllers.
5. Write a C program to blink LEDs on ARM Controller board.
6. Develop a system to rotate a stepper motor by 180^0 when temperature is above set threshold.

7. Develop a system to rotate a DC motor with different rpm depending upon temperature.
8. Implement Communication protocol on ARM Controllers.
9. Local processing on the sensor nodes
10. Develop a sample IoT application by connecting devices to the cloud and vice Versa

Reference Books:

1) Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd Edition, Newnes, (Elsevier), 2010.
2) Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2nd edition.
3) James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
4) Yifeng Zhu, “Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language andC”, 2nd E -Man Press LLC ©2015
5) Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003.

21UECL605	Minor Project-II	(0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

Minor project-II focuses on an exposure to the project work in the domain of their interest by selecting a problem definition from an emerging area. The problem could be defined to develop prototypes for industrial needs.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** and **justify** the technical aspects of the chosen project with a comprehensive and systematic approach.	1	2,4	6,7
CO-2	**Reproduce** and **refine** technical aspects for engineering projects.	2	13	-
CO-3	**Work** as an individual or in a team in development of projects	9	8	-

CO-4	**Implement** the solution in hardware and / or software	3,5	13,14	11
CO-5	**Present** the work in a systematic manner	10	12	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	2.5	3	2	3	1	1	2	3	3	1	2	2	2

Prerequisites: Knowledge of VLSI, Signal Processing, Analog& Digital Communication and Any Programming Language

Guidelines for Conduction Spirit of the Course:

To ensure that undergraduates successfully apply the knowledge they have gained in different courses and integrate material learnt at different stages of the curriculum up to the 5th semester so as to complete the project work within the stipulated time duration following guidelines are framed:

1. Project groups are formed with 3-4 students in each team.
2. Project coordinators instruct student project batches to submit synopsis in the prescribed format in the field of their choice.
3. Project coordinators allot guides based on their field of specialization. However students can have further discussions on the project topic and can modify their project title.
4. Students are instructed to report to their respective guides on weekly basis for discussion.
5. Students are instructed to maintain separate project diary/notebook to show the progress work while having discussion with guide and review committee members.
6. Two reviews are fixed in a semester to monitor the progress of the project.

Assessment: CIE: Project guides evaluate for 30 marks and 20 marks are allotted by reviewers conducting two reviews. 50 marks allotment under CIE. **SEE:** Minor project-II has SEE component and marks allotted for SEE is 50, where students need to demonstrate the project and present it in the presence of examiners.

Note:

- Designated committee is constituted with 2-4 committee members to monitor the process of Minor Project-II

- An internal guide is allotted per group who guides and monitors the project progress.
- Problem statements can be derived from industry, society, etc., after interacting with them.
- Course outcomes (4 or more) are written and mapped to program outcomes and program specific outcomes. In addition to that other POs can also be included if those POs are deemed suitable.
- At the end of the course, students are required to document the project in the form of report.

21UHUL606	Soft skills and Aptitude	(0-0-2)1

Contact Hours: 24

Course Learning Objectives (CLOs):

This is included with the objectives of improving the communication skills, proficiency in English language and aptitude ability of the student to enhance the employability.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the significance of communication in the profession.	-	10	-
CO-2	**Use** the English language with proficiency	-	10	12
CO-3	**Solve** Aptitude related problems	-	9	12
CO-4	**Demonstrate** the competency in the placement activities.	-	9	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	2.0	2.0	-	1.0	-	**-**

Contents:

Training on communication skills, proficiency in English language Analytical Puzzles ▪ Classification Puzzles ▪ Mathematical Puzzles ▪ Human Relations ▪ Directional tests ▪ Coding and decoding ▪ Series completion – Verbal and Non-verbal **06 Hrs**

Number System, Linear Equations + Assessment Test ▪ HCF and LCM, Ratios & Proportions + Assessment Test ▪ Percentage, Profit & Loss + Assessment Test ▪ Time, Work & Distance + Assessment Test **06 Hrs**

Simple and compound Interest, Averages and Mixtures + Assessment Test ▪ Permutations, Probability + Assessment Test ▪ Data analysis **06 Hrs**

Understanding Discussions ▪ Parameters measured in GDs ▪ Video Analysis of GDs ▪ Knowledge base and Ideas ▪ Taking the initiative **06 Hrs**

Evaluation:

Both the internal and external resource persons shall be engaged in imparting the related knowledge and shall have only CIE as the evaluation component. There shall be one test conducted at the end for 25 marks in Aptitude testing and there shall be one presentation by the student for 25 marks or any other suitable testing components. The arrangement for CIE evaluation is to be done by the department and maintain the relevant documents.