Academic Program: PG

Academic Year 2024-25

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

I Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for I semester M.Tech in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering &Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2024-25 tillfurther revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION:

To develop competent professionals with human values.

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives(PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and life long learning in the broadest context of technological changes.

Scheme for I Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
24PDEC100	Applied Mathematics	3-0-0	3	50	100	3	-	-
24PDEC101	Digital System Design Using Verilog	3-0-0	3	50	100	3	-	-
24PDEC102	Sequential Machines and Fault Analysis	3-0-0	3	50	100	3	-	-
24PDEC103	Digital VLSI Design	3-0-0	3	50	100	3	-	-
24PDEC104	Nano Electronics	3-0-0	3	50	100	3	-	-
24PRMC105	Research Methodology and IPR	2-0-0	2	50	100	3	-	-
24PDEL101	Digital Circuits Simulation Laboratory	0-0-2	1	50	-	-	50	3
Total		**17-0-2**	**18**	**350**	**600**		**50**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

* SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

I – Semester

24PDEC100	Applied Mathematics	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs): This course will enable students to acquaint with principles of Probability theory, Random process, Linear Algebra, Wavelet transforms Laplace transform and Linear programming problems and apply the knowledge in the applications of Electronics and Communication Engineering Sciences.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in random processes.	-	1,2	-
CO-2	Learn the concept of Wavelets and its Applications to Denoising.	-	1,2	-
CO-3	Apply Linear Algebra, QR and singular value decomposition techniques for data compression, least square approximation in solving inconsistent linear systems.	-	1,2	-
CO-4	Apply transform method to solve one-dimensional wave equation, one-dimensional heat equation, Laplace equation, Poisson equation.	-	1,2	-
CO-5	Solve system of linear and non-linear equation arising in engineering fields	-	1,2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	2.0	-	-	-	-

Pre-requisites: Basics of Probability, Differentiation and Integration, Vectors.

Contents:

1) Probability Theory: Review of basic probability theory. Definitions of random

variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions example. **09 Hrs**

2) **Introduction to Wavelets Theory:** Introduction, The origin of wavelets, wavelets and other reality transforms. Wavelets in future. Continuous Wavelets: First level of introduction of wavelet transforms. Continuous time frequency representation of signals. Discrete Wavelet Transform signal decomposition (Analysis) frequency response, signal reconstruction. Applications of Wavelets in science and Engineering.

   Denoising: Introduction, Denoising using wavelet shrinkage – statistical modelling and estimation, Noise estimation, Denoising Images with MATLAB. **10 Hrs**

3) **Transform Methods:** Laplace transform methods for one dimensional wave equation–Displacement sina string–Longitudinal vibration of elastic bar, Fourier transform methods for one dimensional heat conduction problems. Fourier transform methods for Laplace equation and Poisson equation. **10 Hrs**

4) **Linear and Nonlinear Programming:** Simplex Algorithm-Two Phase and Big M techniques - Duality theory - Dual Simplex method, Nonlinear Programming – Constrained extremal problems - Lagranges multiplier method Kuhn -Tucker conditions and solutions. **10 Hrs**

Reference Books:

1) Richard Bronson, "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2) Venkataraman M K, " Higher Engineering Mathematics", National Pub.Co,1992.
3) Sneddon, I. N., "Elements of partial differential equations", Dover Publications, 2006.
4) Taha H A, "Operations research- An Introduction", Mc Milan Publishing Co, 1982.
5) K. P. Soman, K.I. Ramachandran, G. Resmi, "Insight into Wavelets (From theory to Practice)", PHI Publications, 3rd edition. 2010.

24PDEC101	Digital System Design using Verilog	(3-0-0)3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on design of various combinational and sequential circuits and design methodology. It also discusses the implementation of advanced digital circuits on programmable devices of varied complexity.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the basic concepts of digital system design using verilog.	-	4	-
CO-2	**Design** the real life applications using verilog.	4	5	1
CO-3	**Design** and **Model** various sequential circuits and memories using verilog.	4	5	-
CO-4	**Describe** various programmable Logic Devices.	-	5	-
CO-5	**Design** processors and controllers using Verilog, for embedded applications.	5	-	6
CO-6	**Elaborate** different I/O devices and fault modeling techniques.	-	-	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	-	2.66	2.25	1

Pre-requisites: Digital Circuit Design, HDL Programming using verilog

Contents:

1) **Introduction and Methodology**: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **08 Hrs**

2) **Sequential Basics**: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology. **08 Hrs**
3) **Memories**: Concepts, Memory Types, Error Detection and Correction. **05 Hrs**
4) **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **05 Hrs**
5) **Processor Basics**: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **04 Hrs**
6) **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **05 Hrs**
7) **Design Methodology**: Design flow, Design optimization, Design for test. **04 Hrs**

Reference Books:

1) Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using Verilog”, Elsevier, 2010.
2) Charles H. Roth, Jr., LizyKurian John, ByeongKil Lee, “Digital Systems Design Using Verilog”, 1/e, Cingage Learning, 2014.
3) Samir Palnitkar, “Verilog HDL”, 2/e, Pearson Education, IEEE 1364-2001Compliant, 2015.
4) Nazeih M Botros, “HDL Programming, VHDL and Verilog”, Dreamtech Press, 2007.

24PDEC102 Sequential Machines and Fault analysis (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on threshold logic, fault detection and location in combinational circuits. It also covers the detailed sequential machine minimization procedures, state assignments using partitions, machine decomposition, state identification and fault detection experiments for sequential machines.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design** of switching circuits by threshold elements	-	4,5	1
CO-2	**Explain, analyze** and **design** of different fault detection and fault	4,5	3	-

	location experiments for combinational logic circuits and sequential machines.			
CO-3	**Analyze** different techniques of failure tolerant design	-	3,4	-
CO-4	**Analysis and application** of algorithms for simplification of completely and incompletely specified sequential machines.	-	5	2,6
CO-5	**Choose** and **adapt** techniques to decompose the sequential machine into series components, parallel components and to achieve input independency, reduction in the output dependency	4,5	-	2,6
CO-6	**Design** and **Implement** homing experiments, distinguishing experiments and machine identification experiments.	-	-	4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2	2	2.2	2.5	1

Pre-requisites: Boolean Algebra, Logic Design

Contents:

1) **Threshold Logic:** Introductory Concepts, Synthesis of Threshold Networks. **07 Hrs**
2) **Reliable Design and Fault Diagnosis Hazards:** Hazards, Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure Tolerant Design, Quadded Logic. **08 Hrs**
3) **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite - State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. **08 Hrs**
4) **Structure of Sequential Machines:** Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of

the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines. **08 Hrs**

5) **State-Identifications and Fault-Detection Experiments:** Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences. **08 Hrs**

Reference Books:

1) Zvi Kohavi, "Switching and Finite Automata Theory", 2nd Edition. Tata McGraw Hill Edition.
2) Charles Roth Jr., "Digital Circuits and logic Design", Thomas Asia Pvt Ltd., Singapore, 6th Edition, 2004.
3) Parag K Lala, "Fault Tolerant And Fault Testable Hardware Design", Prentice Hall Inc. 1985
4) E. V. Krishnamurthy, "Introductory Theory of Computer", Macmillan Press Ltd, 1983.
5) Mishra & Chandrasekaran, "Theory of computer science Automata, Languages and Computation", 2nd Edition, PHI, 2004.

24PDEC103	Digital VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on understanding the construction details and electrical characteristics of MOSFETs, designing different digital applications of MOSFETs for the high speed and low power considerations.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction and the characteristics of MOS structures.	-	-	5

CO-2	**Design** of an Inverter with different loads.	-	4,5	-
CO-3	**Design** digital circuits using various design styles.	4,5	-	6
CO-4	**Discuss** Bi-CMOS gates and **Compare** the performance of CMOS and Bi-CMOS logic circuits.	4,5	6	-
CO-5	**Explore** various memory structures and low power design techniques.	-	4,5	-
CO-6	**Design** and Validate performance of digital systems.	4,5	1,3,6	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	1	2	2.6	2.6	1.6

Pre-requisites: Digital Circuit Design, Basic VLSI Design

Contents:

1) **MOS Field Effect Transistors (MOSFETs):** Device structure and physical operation, Current voltage characteristics, MOSFET circuits as DC, MOSFET as an amplifier and switch, Biasing in MOS Amplifier circuits. **08 Hrs**
2) **MOS Inverters:** Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter. MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints. **06 Hrs**
3) **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **06 Hrs**
4) **Semiconductor Memories**: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Non-volatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). **06 Hrs**
5) **Low-Power CMOS Logic Circuits:** Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits. **06 Hrs**

6) **Bi-CMOS Logic Circuits:** Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behaviour of BJTs, Basic Bi-CMOS Circuits: Static Behaviour, Switching Delay in Bi-CMOS Logic Circuits, Bi-CMOS Applications. **07 Hrs**

Activity beyond syllabus: Design of Digital Circuits using Cadence Software.

Reference Books:

1) Sung Mo Kang &Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition,2003.
2) Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd., 2000.
3) Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies" Kluwer Academic, 2010.
4) ADEL Sedra, Kenneth C Smith, "Microelectronic Circuits Theory & Applications," Oxford Publication, 2013.

24PDEC104	Nano Electronics	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the study of various nanostructures, their properties and applications. The course also focuses on understanding the physical, chemical and fabrication aspects of nanostructures and nanodevices at nanoscale, relevant to the field of electronics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Realize** the significance of Nanoelectronics, as an emerging area in the field of electronics.	3	-	-
CO-2	**Identify** various nanostructures, discuss their properties and applications	-	4	-
CO-3	**Analyze** and **discuss** the physical	4	-	5

	effects occurring in various nanodevices.			
CO-4	**Classify** different microscopic techniques required to study novel properties of nanostructures occurring at nanoscale.	-	4	-
CO-5	**Compare** and **differentiate** various quantum structures, self assembly techniques.	-	-	1
CO-6	**Discuss** the applications of nanostructures, in relevance to the field of electronics.	3	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	3	2.3	1	1

Pre-requisites:
Physics, Electronics, Engineering Mathematics, Material Science

Contents:

1) **Introduction:** Overview of nanoscience and engineering, Development milestones in microfabrication and electronic industry. Moore‘s law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale. Fabrication methods: Top down processes, Bottom up processes, methods describing the growth of nanomaterials, ordering of nanosystems. **08 Hrs**
2) **Characterization:** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques. **07 Hrs**
3) **Inorganic semiconductor nanostructures:** Overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.
4) **Carbon Nanostructures:**Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **08 Hrs**

5) **Fabrication techniques:** Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching. Strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.
   Physical processes: Modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural. **08 Hrs**
6) **Nanosensors:** Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future.
   Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures. **08 Hrs**

Reference Books:

1) Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2) Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology” , John Wiley, Copyright 2006, Reprint 2011.
3) T Pradeep, “Nano:The essentials-Understanding Nanoscience and Nanotechnology”, TMH.
4) Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “ Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

24PRMC105	Research Methodology and IPR	(2-0-0) 2

Contact Hours: 26

Course Learning Objectives (CLOs): The students are expected to learn about the need and types of research, problem formulation, literature review, measurement, scaling, data collection, testing of hypothesis, result interpretation and report writing. Further, the students shall know about the intellectual property rights, copy rights, trademarks, patents, patents filing procedure, infringement & remedies and information technology act etc.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Formulate** the research problem, carryout literature survey and decide the methodology.	-	1	-
CO-2	**Use** measurement and scaling and **carryout** data collection.	-	1	-
CO-3	**Test** the hypothesis, **interpret** & **analyze** the results and **write** the report.	2	3	-
CO-4	**Explain** the need of IPR, copy right, patents, trademarks & the filing procedure and know about infringement, remedies and regulatory framework.	-	2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2.5	2	-	-	-

Pre-requisites: Branch specific course on problem analysis (Preferred)

Contents:

1) **Research Methodology:** Introduction, meaning of research, objectives of research, motivation in research, types of research, research approaches, research process, criteria of good research and problems encountered by researchers in India.

   Defining the Research Problem: Research problem, selecting the problem, technique involved in defining a problem, an illustration. **4 Hrs**

2) **Reviewing the literature:** How to review the literature, searching the existing literature, reviewing the selected literature.

   Research Design: Meaning of research design, need for research design, features of a good design, important concepts relating to research design, different research designs. **4 Hrs**

3) **Measurement and Scaling:** Measurement in research, measurement scales,

sources of error in measurement.

Data Collection: Collection of primary data, collection of secondary data. **4 Hrs**

4) **Testing of Hypotheses:** What is a Hypothesis? Basic concepts concerning testing of hypotheses, procedure for hypothesis testing, flow diagram for hypothesis testing, measuring the power of a hypothesis test, tests of hypotheses. **4 Hrs**
5) **Interpretation and Report Writing:** Meaning of interpretation, technique of interpretation, precaution in interpretation, significance of report writing, different steps in writing report, layout of the research report, precautions for writing research reports, plagiarism and its significance. **3 Hrs**
6) **Introduction to Intellectual Property Rights:** Meaning and conception of IPR, competing, rationale for protection, international conventions, world court.

Copy right: Meaning, content, substance, ownership, primary, special rights, obligations, period, assignment, and relinquishment of copy rights. License and application for registration of copy right.

Patents: Meaning of Patent, purpose and policy object of patent law, gains to inventor, application of patents, joint application, discovery and invention, patentable and non-patentable inventions.

Industrial design: Concepts & Significance

Trademarks: Definitions and conceptions of Trademark, advantages of registration, marks which are not registrable, known, and well-known trademarks, application for registration and procedure for registration, procedure, and certification of Trademarks.

Infringement and Remedies: Meaning of infringement, acts of infringement.

7 Hrs

Self Study:

The Information Technology Act: Definitions, certifying authority, meaning of compromise of digital signature, offences and penalties, applicability of IPRs, cybercrimes, adjudicating officer, violation, damages and penalties, Cyber regulation appellate tribunal, World Wide Web and domain names and cyber flying, Self study.

Reference Books:

1) C.R. Kothari, Gaurav Garg, Research Methodology: Methods and Techniques, New Age International, 4th Edition, 2018.
2) Ranjit Kumar, Research Methodology a step-by-step guide for beginners,

SAGE Publications, 3rdEdition, 2011.

3) Fink A, Conducting Research Literature Reviews: From the Internet to Paper, Sage Publications, 2009.

4) N. K. Acharya, Text book on Intellectual Property Rights,4th Edition, Asia Law House, Hyderabad.

24PDEL101 Digital Circuits Simulation Laboratory (0-0-2)1

Contact Hours:24

Course Learning Objectives (CLOs):

The course focuses on design of digital circuits and verifying the same by using LabVIEW and Verilog code. The experiments are meant to give a good understanding of tools for realization of digital systems.

Course Outcomes (COs):

Description of the course outcomes: At the end of the course the students will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Demonstrate** logic gate **implementation** using Verilog code.	-	4	-
CO-2	**Design** different digital circuits and **verify** the functional simulation.	3	5	-
CO-3	**Design** a digital system for addition and multiplication operations.	3	-	-
CO-4	**Implement** sequential digital circuits on FPGA board.	3	4	-
CO-5	**Develop** LIFO and FIFO systems.	3	4	-
CO-6	**Build** and **Implement** application based digital system as a part of Hobby Projects.	3,4	1,2,5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	3	2.25	2	1

Prerequisites: Digital Electronics, Verilog HDL

Contents:

Write Verilog codes to implement Digital circuits on FPGA/CPLD boards and performance testing may be done using pattern generator, Chip scope pro apart from verification by simulation with any of the frontend tools.

1) Write a Verilog code for 8:1 multiplexor in behavioral model, data flow and structural model.

2) Write a Verilog code for D and J-K FF using blocking and non- blocking statements.

3) Write a Verilog code for one bit full adder / subtractor.

4) Write Verilog code for the design of 8-bit.

i. Carry Ripple Adder

ii. Carry Look Ahead adder

iii. Carry Skip Adder

5) Write Verilog Code for 8-bit

i.Array Multiplication

ii.Booth Multiplication (Radix-4)

6) Write Verilog code for 4/8-bit

a. Magnitude Comparator

b. LFSR

7) Write Verilog Code for 3-bit arbitrary counter to generate 0,1,2,3,6,5,7 and repeats.

8) Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg11101 (with and without overlap) any sequence can be specified.

9) Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

10) Write Verilog code to implement 8-bit ALU with arithmetic and logical operations.

Reference books:

1) Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using Verilog”, Elsevier, 2010.

2) Charles H. Roth, “Fundamentals of logic design”, Thomson Learning, 2004.

3) NCLaunch User Guide Product Version 3.1 June 2000.

4) NC Verilog Simulator Help Product Version 3.1 June 2000.