Academic Program: PG

Academic Year 2023-24

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

III & IV Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

Ph: 0836-2447465 **Fax: 0836-2464638** **Web: www.sdmcet.ac.in**

SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for III &IV semester M.Tech in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering &Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2023-24 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION

To develop competent professionals with human values.

MISSION

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives(PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self-confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and lifelong learning in the broadest context of technological changes.

Scheme for III Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
22PDEC300	VLSI for Signal Processing	4-0-0	4	50	100	3		
22PDEE35X	Elective 5	3-0-0	3	50	100	3		
22PDEE35X	Elective 6	3-0-0	3	50	100	3		
22PDEE35X	Elective 7	4-0-0	4	50	100	3	--	--
OR								
22PDEL300	**Internship in Industry or R&D organization	Min 4 weeks during vacation after 2nd sem	4	50	--	--	100	3
22PDEL301	***Project Phase-I	0-0-6	6	50			50	3
Total		**14-0-6/10-4 weeks-6**	**20**	**250**	**400/ 300**		**50/150**	

Course Code	Course Title	Credits
22PDEE350	Advances in VLSI Design	3
22PDEE351	Error Control Coding	3
22PDEE352	Wireless Sensor Networks	3
22PDEE353	Image and Video Processing	3
22PDEE354	Advanced DSP	4
22PDEE355	Block Chain Technology	3
22PDEE356	Advanced Computer Architecture	4
22PDEE357	Real Time Operating Systems	3

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

***SEE** for theory courses is conducted for 100 marks and reduced to 50 marks.

****Internship**: The students are expected to undergo training in industry for a period of ***four weeks*** during the vacation immediately after completion of II Semester examination. A faculty is to be allotted to guide the student. A committee consisting of three faculty members shall evaluate the work carried out and the knowledge the students have acquired. **OR students can take one elective course if they do not undergo internship.**

*****Project Phase-I: The students are expected to formulate the problem and carry out the intensive literature survey along with preliminary investigations supporting the project phase-II in IV semester.

Scheme for IV Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
22PDEL400	**Project Phase-II	0-0-22	18	100	--	--	100	3
22PDEEOA1	***BOS recommended ONLINE course	-	Audit (PP)	-	-	-	-	-
22PDEEOA2	***BOS recommended ONLINE course	-	Audit (PP)	-	-	-	-	-
Total		**0-0-22**	**18**	**100**	**--**	**--**	**100**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

- SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

** Project Phase-II: The students are expected to work on a project for the full semester in an industry or an institution

*** Classes and evaluation procedures are as per the policy prescribed for online courses by the institution.

Total Credits offered for the first year: 42
Total Credits offered for the Second year: 38

III Semester

22PDEC300	VLSI for Signal Processing	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The subject focuses on several high level architectural transformations that can be used to design families of architectures for a given algorithm and develop knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** high-level architectural transformation for effective integrated circuit implementations	4	3	6
CO-2	**Analyze** high-level algorithmic transformation for effective integrated circuit implementations	4	3	6
CO-3	**Explain and apply** arithmetic strength reduction techniques	5	3	-
CO-4	**Explain and apply** numerical strength reduction techniques	5	3	-
CO-5	**Compare** the techniques of reducing the computational complexity	4	-	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	3	3	1

Pre-requisites: Digital Signal Processing, VLSI design

Contents:

1) **Introduction to Parallel Processing:** Parallelism in uniprocessor systems, Parallel Computer structures, architectural classification schemes, Parallel Processing Applications. Principles of Pipelining and Array Processors, an overlapped parallelism, instruction and arithmetic pipelines, data buffering and busing structures, SIMD array processors, parallel algorithm for array Processors. **08 Hrs**

2) **Iteration Bound, Pipelining, Parallel Processing, Retiming**: Introduction, Data-Flow graph representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power, Retiming Definitions and properties, solving systems of inequalities, Retiming Techniques. **09 Hrs**
3) **Unfolding and Folding**: Introduction, An algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, Applications of unfolding, folding transformation, register minimization techniques, register minimization in folded architectures, folding of multi-rate systems. **08 Hrs**
4) **Algorithmic Strength Reduction in filters and Transforms:** Introduction, Parallel FIR filters, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for Rank-Order filters. **09 Hrs**
5) **Pipelined and Parallel Recursive filters**: Introduction, pipeline interleaving in digital filters, pipelining in 1^{st}order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low-power IIR Filter Design using pipelining and parallel processing. **09 Hrs**
6) **Redundant Arithmetic and Numerical Strength Reduction:** Introduction, Redundant number representations, carry-free radix-2 addition and subtraction, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architectures, data format conversion, sub-expression elimination, multiple constant multiplication, sub-expression sharing in digital filters, additive and multiplicative number splitting. **09 Hrs**

Reference Books:

1) Kai Hwang & Faye A. Briggs, “Computer Architecture and Parallel Processing” McGraw-Hill Series, 1984.
2) Parhi, K.K., “VLSI Digital Signal Processing Systems: Design and Implementation”, John Wiley, 2007.
3) Wanhammar, L., “DSP Integrated Circuits”, Academic Press, 1999.
4) Magdy A. Bayoumi, “VLSI Design Methodologies for Architectures”, Kluwer Academic Publishers, 1994.
5) Mitra, S.K., “Digital Signal Processing: A Computer Based Approach”, McGraw Hill, 2007, 3rd edition.

22PDEE350	Advances in VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the theory and design principles of VLSI devices and circuits. The course concentrates on the study and analysis of various combinational and sequential MOS logic circuits for VLSI applications.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction, characteristics and various processes involved in the CMOS technology.	-	-	4
CO-2	**Discuss** the construction and working of MESFETS, MIS structures and MODFETS.	-	4	-
CO-3	**Apply** rules involved in the schematic and layout design for VLSI circuits.	4	5,6	2
CO-4	**Explain** CMOS circuits with respect to different technologies.	-	4,5	-
CO-5	**Identify and describe** the challenges involved in digital CMOS VLSI design.	-	3,4	5,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	1	2	2	1.6	1.5

Pre-requisites: Analog Electronics, Network Analysis, Digital Circuits.

Contents:

1) **Review of MOS Circuits:** MOS and CMOS static plots, switches, comparison between CMOS and Bi - CMOS. **04 Hrs**
2) **MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS. **05 Hrs**
3) **MIS Structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. **05 Hrs**

4) **Super Buffers, Bi-CMOS and Steering Logic:** Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks–NMOS and CMOS functional blocks. **08 Hrs**
5) **Special Circuit Layouts Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR-NOR, and AOI Logic, NMOS,CMOS Multiplexers, Barrel shifter, Wire routing and module layout. **09 Hrs**
6) **System Design:** CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom design. Beyond CMOS. **08 Hrs**

Reference Books:

1) Kevin F. Brennan, "Introduction to Semiconductor Device", Cambridge University publications, 2005.
2) Eugene D. Fabricius, "Introduction to VLSI Design", McGraw-Hill International publications,1990.
3) D. A. Pucknell, "Basic VLSI Design", PHI Publication, 2001.
4) Wayne Wolf, "Modern VLSI Design" Pearson Education, Second Edition, 2002.

22PDEE351 Error Control Coding (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on various error detection and error correction coding techniques.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain and Analyze** Linear block codes, cyclic codes.		2	
CO-2	**Explain and Analyze** BCH Codes and Majority Logic Decodable Codes.		1	3
CO-3	**Explain** and **analyze** convolution		2	

	codes, Concatenated, Turbo, LDPC codes and burst error correcting codes.			
CO-4	**Design** and **Implement** different error control codes.	4		5,6
CO-5	**Choose** and **adapt** error control coding techniques for different applications.		1	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	2	3	1	1

Pre-requisites: Information Theory & coding, Digital Communication

Contents:

1) **Linear Block Codes:** Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Hamming Codes, Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes. **06Hrs.**
2) **Cyclic Codes:** Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes – Encoding using Feedback shift register circuits, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, (23, 12) Golay code, Shortened cyclic codes. **10 Hrs**
3) **BCH Codes and Majority Logic Decodable Codes :** Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Reed – Solomon Codes, One – Step Majority logic decoding, one – step Majority logic decodable Codes. **09 Hrs**
4) **Convolution Codes:** Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Stack and Fano sequential decoding Algorithms. **08 Hrs**
5) **Concatenated Codes & Turbo Codes:** Single level Concatenated codes, Multilevel Concatenated codes, Introduction to Turbo coding and their distance properties, Introduction to LDPC Coding. **06 Hrs**

Activity beyond Syllabus: Assignments on the design of various coding techniques.

Reference Books:

Shu Lin & Daniel J. Costello, Jr. "Error Control Coding", Pearson / Prentice

1) Blahut R. E R.E., "Theory and Practice of Error Control Codes", Addison Wesley, 1984.

2) Satyanarayana P.S., "Concepts of Information Theory & coding", DynaramPublications, Bangalore, 2005.

3) Ranjan Bose, "Information Theory, Coding and Cryptography", Tata McGraw-Hill Publication, 2002, ISBN: 0-07-048297-7

22PDEE352	Wireless Sensor Networks	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on architecture of Wireless sensor nodes, Operating systems used in WSN, Medium Access Control Protocols, Networks Protocols, Power Management, Time Synchronization, Localization and security issues in WSN.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** various parts of WSN and **explain** their construction and operation	3	-	-
CO-2	**Apply** suitable medium access control technique for a given application of WSN.	3	1	-
CO-3	**Apply** suitable data dissemination and routing protocol for a given application of WSN.	4	5	1
CO-4	**Apply** various techniques and **solve** the problems related to power efficiency and synchronization in WSN	-	4	1
CO-5	**Apply** the techniques and **determine** solutions various issues related to localization and security issues in WSN	-	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.33	-	3	2.4	2	1

Pre-requisites: Sensors and Actuators, Wireless Communication, Microcontrollers, Communication Network protocols.

Contents:

1) **Wireless Sensor Network Basics**: Motivation, Definitions and Background, Challenges and Constraints, Areas of Applications, Node Architecture, Sensing Subsystem, Processor Subsystem, Communication Interfaces, Operating Systems, Functional and Non functional aspects of OS. **05 Hrs**
2) **Medium Access Control:** Medium Access Control, Overview, Wireless MAC Protocols, Characteristics of MAC Protocols in Sensor Networks, Contention-Free MAC protocols, Contention based MAC protocols, Hybrid MAC protocols. **08 Hrs**
3) **Network Layer**: Overview, Routing Metrics, Flooding and Gossiping, Data-centric Routing, Proactive Routing, On-Demand Routing, Hierarchical Routing, Location based Routing, QoS based routing protocols. **08 Hrs**
4) **Power Management and Time Synchronization:** Local Power Management Aspects, Dynamic Power Management, Conceptual Architecture, Clocks and synchronization problem, Time synchronization in WSN, Basics of Time synchronization, Time synchronization protocols. **09 Hrs**
5) **Localization and Security:** Overview, Ranging Techniques, Range based Localization, Range-Free Localization, Event Driven Localization, Fundamentals of Network Security, Challenges of Security in WSN, Security Attacks in Sensor Networks, Protocols and Mechanisms for Security. **09 Hrs**

Reference Books:

1) Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks”, Wiley Publications, 2014.
2) Kazem Sohraby, Daniel Minoli, Taieb Znati “Wireless Sensor Networks”, Wiley Publications, 2015.
3) Jun Zeng, Abbas Jamalipour "Wireless Sensor Networks", Wiley Publications, 2014.
4) S. Swapnakumar, "A Guide to Wireless Sensor Networks”, Laxmi Publications, 2013.

22PDEE353	Image and Video Processing	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on image sampling, quantization, various image enhancement techniques, color image processing, image compression and fundamental concepts in video processing. The course also discusses various applications of image processing.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to PO (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** image sampling, quantization and model of color vision.	-	-	2
CO-2	**Apply** suitable image enhancement and restoration techniques.	-	4, 3	2
CO-3	**Differentiate** various filtering techniques in image processing.	-	3	2,1
CO-4	**Choose** appropriate feature extraction technique in analyzing the given image.	3	4	1
CO-5	**Select** appropriate image reconstruction algorithms and video processing techniques.	3	2	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	1.25	2.5	2.0	-	-

Pre-requisites: Digital signal processing**,** Stochastic and random process.

Contents:

1) **Image Perception:** Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision.

04 Hrs

2) **Image Sampling and Quantization:** Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. **05 Hrs**
3) **Image Enhancement:** Point operations, Histogram modeling, Spatial operations, Transform operations, Multi-spectral image enhancement, False color and pseudo-color, Color Image enhancement. **06 Hrs**
4) **Image Filtering & Restoration:** Image observation models, Inverse & Wiener filtering, Fourier domain filters, Smoothing splines and interpolation, Least squares filters, Generalized inverse, SVD and iterative methods, Maximum entropy restoration, Bayesian methods. **06 Hrs**
5) **Image Analysis & Computer Vision:** Spatial feature extraction, Transform features, Edge detection, Boundary extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification techniques. **06 Hrs**
6) **Image Reconstructions from Projections:** Introduction, Radon transform, Back projection operator, Projection theorem, Inverse Radon transform, Convolution/ Filter back-projection algorithm. **06 Hrs**
7) **Video Processing:** Fundamental concepts in video – Types of video signals, Analog video, Digital video, Color models in video, Video compression techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. **06 Hrs**

Activity beyond Syllabus: Seminar, Simulation based project.

Reference Books:

1) Anil K. Jain, “Fundamentals of Digital Image Processing," Pearson Education (Asia) Pvt. Ltd., Prentice Hall of India, 2004.
2) Z. Li and M.S. Drew, “Fundamentals of Multimedia”,Pearson Education (Asia)Pvt. Ltd., 2004
3) R. C. Gonzalez and R. E. Woods, “Digital Image Processing”, 2nd edition, Pearson Education (Asia) Pvt. Ltd, Prentice Hall of India, 2004.
4) M. Tekalp, “Digital Video Processing”, Prentice Hall, USA, 1995.
5) K. P. Soman, “Digital Signal & Image Processing’, 1st edition, Elsevier India, 2012.

22PDEE354	Advanced DSP	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on some of the modern techniques in signal processing such as multi rate signal processing, signal transforms and nonlinear filters and adaptive filters.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze and outline** the principles of multirate signal processing techniques	1, 5	-	-
CO-2	**Apply** multirate concepts for various applications of signal processing	-	2	6
CO-3	**Analyze** the principles of nonlinear digital filters and **Evaluate** the output of nonlinear digital filters.	3, 5	-	6
CO-4	**Analyze** adaptive filtering techniques and their applications	1, 4	2	-
CO-5	**Explain** the concepts, mathematical representations and applications of Wavelet transforms	4	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3.0	2.0	3.0	3.0	2.7	1.0

Pre-requisites: Digital Signal Processing

Contents:

1) **Fundamentals of Multirate Systems**: Introduction, Basic Multirate Operations, Interconnection of Building Blocks, The Polyphase Representation, Multistage Implementations, Applications of Multirate Systems. **10 Hrs**

2) **Maximally Decimated Filter Banks:** Introduction, Errors created in the QMF Bank, A Simple Alias Free QMF System, M-Channel Filter Banks, Polyphase Representation, Perfect Reconstruction Systems, Alias Free Filter Banks, Applications. **10 Hrs**
3) **Nonlinear Digital Filtering:** Trimmed Mean Filters, L-Filters, C-Filters, Weighed Median Filters, Ranked-Order and Weighed Order Statistic Filters, Multistage Median Filters, Median Hybrid Filters, Edge-Enhancing Selective Filters, Rank Selection Filters, M-Filters, R-Filters, Nonlinear Mean Filters. **10 Hrs**
4) **Introduction to Adaptive filter:** 3 kinds of estimation, Adaptive filter, Approaches to the development of Linear Adaptive filter, Applications of Adaptive Filters. LMS Adaptive Filters, Overview of the structure & operation of LMS algorithm, LMS algorithm, Summary of the LMS algorithm, Applications of LMS algorithm. RLS Adaptive Filters, exponentially weighted recursive least squares algorithm, selection of the regularization parameter, update recursion for the sum of weighted error squares, example single weight adaptive noise canceller. **12 Hrs**
5) **Multiresolution Analysis:** Short-time Fourier transform - Heisenberg uncertainty principle, Principles of multi-resolution analysis - sub-band coding, the continuous and discrete wavelet transform - properties. Applications of wavelet transform - noise reduction, image compression. **10 Hrs**

Reference Books:

1) P.P. Vaidyanathan, “Multirate systems and filter banks” Prentice Hall, 1993.
2) Jaakko Astola, Pauli Kuosmanen, Fundamentals of Nonlinear Digital filtering, CRC Press.
3) Simon Haykin, Adaptive Filter Theory, 4th Edition, Pearson Education.

22PDEE355	Block Chain Technology	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on understanding emerging abstract models for Blockchain Technology and familiarizes the functional/operational aspects of the crypto currency ecosystem. Identify major research challenges and technical gaps existing between theory and practice in the crypto currency domain.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Demonstrate** the basics of Block chain concepts using modern tools/technologies	-	3,4,5	1,13
CO-2	**Analyze** the role of block chain applications in different domains including cyber security.	-	3,5	-
CO-3	**Evaluate** the usage of Block chain implementation/features for the given scenario.	-	1,3,4	14
CO-4	**Exemplify** the usage of bitcoins and its impact on the economy.	3	-	-
CO-5	**Analyze** the application of specific block chain architecture for a given problem.	3	2	6

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.0	2.4	1.0	2.0	1.0	-	-	-	-	-	-	-	1.0	1.0

Pre-requisites: Knowledge of any Object Oriented Programming language and Data Structures.

Contents:

1. **Introduction:** Introduction to Blockchain, How Blockchain works, Blockchain vs. Bitcoin, Practical applications, public and private key basics, pros and cons of Blockchain, Myths about Bitcoin. **07Hrs**
2. **Blockchain Architecture and Types:** Architecture, versions, variants, use cases, Life use cases of Blockchain, Blockchain vs. shared Database, Introduction to crypto currencies, Types, Applications. **08Hrs**

3. **Blockchain Data Structures and Working:** Concept of Double Spending, Hashing, Mining, Proof of work. Introduction to Merkel tree, Privacy, payment verification, Resolving Conflicts, Creation of Blocks. **08Hrs**

4. **Bitcoins:** Introduction to Bitcoin, key concepts of Bitcoin, Merits and Demerits Fork and Segwits, Sending and Receiving bitcoins, choosing bitcoin wallet, Converting Bitcoins to Fiat Currency. **07Hrs**

5. **Ethereum:** Introduction to Ethereum, Advantages and disadvantages, Ethereum Vs. Bitcoin, Introduction to smart Contracts, usage, application, working principle, Law and regulations, Case study. **09Hrs**

Reference Books:

1) Arshdeep Bikramaditya Singhal, Gautam Dhameja, Priyanshu Sekhar Panda “Beginning Blockchain: A Beginner's Guide to Building Blockchain Solutions” Apress Publications, 2018.
2) Arshdeep Bahga, Vijay Madisetti, “Blockchain Applications: A Hands-On Approach”, VPT Publications, 2017.
3) Swan Melanie, “Blockchain: Blueprint for New Economy”, O’Reilly Publications, 2018.
4) Aravind Narayan, Joseph Bonneau, Edward Felten at al “Bitcoin and Cryptocurrency Technologies: A Comprehensive Introduction” Princeton University Press, 2016.
5) Daniel Drescher, “Blockchain Basics: A Non-Technical Introduction in 25 Steps”, Apress Publications, 2017.

22PDEE356	Advanced Computer Architecture	(4-0-0) 4

Contact Hours: 52Hrs

Course Learning Objectives (CLOs):

The course deals with the understanding quantitative principles guiding the computer system design. It focuses on enhancing the performance by addressing parallelism at different levels such as Instruction, thread, task, job. Evaluates memory hierarchy, speculations, ISA, ALU architectures, choice of I/O is major motivation

Course Outcomes:

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	Understand parallel computing concepts, identify opportunities for parallelism, and grasp principles of scalable performance.	1	5	4
CO-2	Explain processor and memory hierarchy, analyze advanced technologies, and understand memory optimization.	1	3	-
CO-3	Describe bus, cache, and shared memory, and evaluate their impact on data access in parallel systems.	4	2	-
CO-4	Analyze multiprocessor architecture, synchronization, and design scalable systems using latency hiding.	-	1,3	6
CO-5	Comprehend parallel programming model, optimize code for parallelization, and utilize parallel programming tools effectively.	6	1,2	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.4	2	1.3	2	2.5	2

Course Contents:

1) **Theory of Parallelism:** Parallel Computer Models, The State of Computing, Multiprocessors and Multicomputer, Multivector and SIMD Computers, PRAM and VLSI Models, Program and Network Properties, Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws. **12 Hrs**

2) **Hardware Technologies-1:** Processors and Memory Hierarchy, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology. **11 Hrs**
Hardware Technologies-2: Bus, Cache and Shared Memory, Bus systems, Cache Memory Organizations, Shared-Memory Organisations, Sequential and Weak Consistency Models. **10 Hrs**

3) **Parallel and Scalable Architectures:** Multiprocessors and Multicomputers, Multiporcessor system Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers, Message-Passing Mechanisms. Scalable, Multithreaded and Dataflow Architectures: Latency Hiding Techniques, Principles of Multithreading, Fine-Grained Multicomputers, Scalable and Multithreded Architectures, Dataflow and Hybrid Architectures. **10 Hrs**

4) **Software for Parallel Programming:** Parallel Programming Model, Parallel Languages and Compilers, Dependence Analysis of Data Arrays, Code Optimization and Scheduling Loop Parallelization and Pipeline. **09 Hrs**

Reference Books

1) Kai Hwang ,"Advanced Computer Architecture: Parallelism, Scalability, Programmability",1993,McGraw-Hill.
2) John L. Hennessy and David A. Patterson "Computer Architecture A Quantitative Approach",6th edition, 2019,Morgan Kaufmann
3) William Stallings "Computer Organization and Architecture Designing for Performance",11th edition, 2022, Pearson.
4) Hesham El-Rewini, Mostafa Abd-El-Barr "Advanced Computer Architecture And Parallel Processing", 2005, Wiley.

22PDEE357	Real Time Operating Systems	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on concepts of real-time systems, computing required for the real-time embedded systems and communication required for the real-time embedded systems.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Understand** the concept of mathematical model of the system.	3	-	1
CO-2	**Describe** real-time algorithm for task scheduling.	-	3,4	2
CO-3	**Understand** the working of real-time operating systems	1	-	-
CO-4	**Analyze** working of real-time database	-	4	5
CO-5	**Describe** the design and development of protocols related to real-time communication	-	5	-

POs	PO1	PO2	PO3	PO4	PO5
Mapping Level	2	1	2.5	2	1.5

Pre-requisites: Operating systems, Embedded systems

Contents:

1) **Introduction:** Introduction to real time systems, Application of real time systems, Basic model of real time systems, characteristics of real time systems, safety and reliability, types of real time tasks, Timing Constraints, Modeling timing constraints. **05 Hrs**
2) **Real Time Task Scheduling:** Some important concepts, Types of real time tasks and their characteristics, task scheduling, clock-driven scheduling, Hybrid schedulers, Event-driven scheduling, Earliest Deadline first scheduling, rate Monotonic algorithm, some issues associated with RMA, issues in using RMA in practical situations. **06 Hrs**
3) **Handling resource sharing and dependencies among real time task:** Resource sharing among real time tasks, Priority inversion, priority inheritance protocol, highest locker protocol, priority ceiling protocol, different types of priority inversion under PCP, important features of PCP, some issues in using a resource sharing protocol, handling task dependencies. **07 Hrs**

4) **Scheduling Real-time tasks in multiprocessor and Distributed systems:** Multiprocessor task allocation, Dynamic allocation of tasks, fault-tolerance scheduling of task, clock in distributed real-time systems, centralized clock synchronization, distributed clock synchronization. **07 Hrs**
5) **Commercial Real-time operating systems:** time services, features of real time operating systems, Unix as a real time operating systems, Unix-based real time operating systems, Windows as a real time operating systems, Portable operating system interface, a survey of contemporary real time operating systems, Benchmarking Real time systems. **07 Hrs**

6) **Real time communications:** examples of real time communication in applications, Basic concepts, Real time communication in LAN, soft real time communication in a LAN, Hard real time communication in a LAN, Bounded Access protocol, performance comparison, real-time communication over internet, Routing Multicast routing, resource reservation, Traffic shaping and policing, Scheduling Mechanism, QoS Models **07 Hrs**

Reference Books:

1) Rajib Mall, Real-Time Systems: Theory and Practice, Pearson Education, 2007
2) C. Siva Ram Murthy and G. Manimaran, 'Resource Management in Real Time Systems and Networks', the MIT Press, 2001
3) C. Mani Krishna, Kang G. Shin, Publisher McGraw-Hill, 1997

22PDEL300	Internship	(4 weeks) 4

Course Learning Objectives (CLOs):

The curriculum has the support for internship to be carried out during vacation immediately after the completion of II semester examination for a minimum period of four weeks in any of the reputed Industries/ Academic Institutes/ R&D Organizations. Students may identify the Industries considering their career choice. The objectives are:

- Internships are intended to provide students with an opportunity to apply theoretical concepts from the classroom to the realities of the field.
- Will expose students to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.
- Provides exposure to the current technological developments relevant to the subject area of training.

- Provides an opportunity to explore and develop their careers through professional practice. Helps students to communicate in a workplace environment in a clear and confident manner and articulate their experience and skills to potential employers.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Acquire** practical experience in an organizational setting	-	1,6	-
CO-2	**Apply** the knowledge and skill set in engineering design processes appropriate to the internship program	1,4	3,5	-
CO-3	**Apply** modern tools and processes to solve the live problems	-	4	-
CO-4	**Get** an opportunity to learn new skills	-	5	-
CO-5	**Learn** strategies like time management, multi-tasking, communication and team work skills in an industrial setup	-	2,5,6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.5	2	2	2.5	2	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field and explore solutions. They are required to know the functions of engineers in managing the floor. Current technological developments, organizational behavior, time management, professional ethics, etc. need to be understood.

2) The above skills obtained need to be documented and presented.

Reference Material:

1) Technical references/research papers
2) Manuals
3) Software packages

20PDEL301	**Project Phase - I**	**(0-0-15) 9**

Contact Hours:100

Course Learning Objectives (CLOs):

The course focuses to encourage innovation, enhance research culture and promote independent learning. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** innovative/research based problem statement through literature survey	1,4,5	-	-
CO-2	**Explore** and **analyze** possible technical solutions for the problem identified	4,5	-	-
CO-3	**Demonstrate** the work progress	3	-	-
CO-4	**Prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in the previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field through literature survey and select a topic from emerging area relevant to the branch.

2) The students are expected to explore and analyze all possible technical solutions for the problem identified and start working on the same using tools.Preliminary design, analysis, simulation etc. is to be done in this phase.

3) The students are expected to document the work done in a systematic way and learn/improve the presentation skills.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools

IV semester

20PDEL400 Project Phase - II (0-0-20) 22

Contact Hours:200

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote team work. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Design** and **Implement** the solution	1,4,5	-	-
CO-2	**Discuss** the outcome of the work	3,4,5	-	-
CO-3	**Justify** the approach and **Integrate** the work carried out by producing technical paper	2,3	-	-
CO-4	**Organize** the topics in a systematic manner and **prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to continue the work providing feasible solutions, justify the approach, defend the same and present the work in national / international conferences or journals.

2) The students are expected to document the work done in a systematic way and deliver the oral presentation.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools