Academic Program: PG

Academic Year 2020-21

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

I & II Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

Ph: 0836-2447465 **Fax: 0836-2464638** **Web: www.sdmcet.ac.in**

SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for I & II semester M.Tech in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2020-21 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION:

To develop competent professionals with human values.

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives(PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and life long learning in the broadest context of technological changes.

Scheme for I Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
20PRMIC100	Research Methodology and IPR	2-0-0	2	50	50	2		
20PMEC100	Applied Mathematics	4-0-0	4	50	100	3		
20PDEC100	Digital Circuits and Logic Design	4-0-0	4	50	100	3		
20PDEC101	Digital System Design Using Verilog	4-0-0	4	50	100	3		
20PDEE15X	Elective 1	4-0-0	4	50	100	3		
20PDEL101	Digital Circuits Simulation Laboratory	0-0-3	2	50			50	3
20PDEL102	Seminar	0-0-2	1	50				
Total		**18-0-5**	**21**	**350**	**450**		**50**	

Elective 1 to 3

20PDEE150	Introduction to Artificial Intelligence & Machine Learning
20PDEE151	Digital Control Systems
20PDEE152	Automotive Electronics
20PDEE153	Nano Electronics

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

***SEE** for theory courses is conducted for 100 marks and reduced to 50 marks.

Seminar is to be conducted every week and 2-3 students/week will present a topic from emerging areas in respective PG program preferably the contents not studied in their regular courses. The seminar shall be evaluated by 3 faculty members having specialization in respective program and allied areas.

Scheme for II Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
20PDEC200	Digital VLSI Design	4-0-0	4	50	100	3		
20PDEC201	Advanced Embedded System Design	4-0-0	4	50	100	3		
20PDEE25X	Elective 2	4-0-0	4	50	100	3		
20PDEE25X	Elective 3	4-0-0	4	50	100	3		
20PDEE25X	Elective 4	4-0-0	4	50	100	3		
20PDEL201	VLSI and Embedded Systems Laboratory	0-0-3	2	50			50	3
20PDEL202	Seminar	0-0-2	1	50				
Total		**20-0-5**	**23**	**350**	**500**		**50**	

20PDEE250	Parallel Computing
20PDEE251	Low Power Circuits and Systems
20PDEE252	Digital Signal Compression
20PDEE253	Artificial Neural Networks and Deep Learning
20PDEE254	IoT Applications
20PDEE255	Coding Theory
20PDEE256	Advanced Mobile Networks
20PDEE257	Software Defined Radio

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

***SEE** for theory courses is conducted for **100 marks** and reduced to **50 marks**.

Seminar is to be conducted every week and 2-3 students/week will present a topic from emerging areas in respective PG program preferably the contents not studied in their regular courses. The seminar shall be evaluated by 3 faculty members having specialization in respective program and allied areas.

I – Semester

20PRMIC100	Research Methodology and IPR	(2-0-0) 2

Contact Hours: 26

Course Learning Objectives (CLOs): The students are expected to learn about the need and types of research, problem formulation, literature review, measurement, scaling, data collection, testing of hypothesis, result interpretation and report writing. Further, the students shall know about the intellectual property rights, copy rights, trademarks, patents, patents filing procedure, infringement &remedies and information technology act etc.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Formulate** the research problem, carryout literature survey and decide the methodology.		1	
CO-2	**Use** measurement and scaling and **carryout** data collection.		1	
CO-3	**Test** the hypothesis, **interpret** & **analyze** the results and **write** the report.	2	3	
CO-4	**Explain** the need of IPR, copy right, patents, trademarks,& the filing procedure and know about infringement, remedies and regulatory framework.		2	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2.5	2	-	-	-

Pre-requisites: Branch specific course on problem analysis (Preferred)

Contents:

1) **Research Methodology:** Introduction, meaning of research, objectives of research, motivation in research, types of research, research approaches, significance of research, research methods versus methodology, research and scientific method, importance of knowing how research is done, research process, criteria of good research and problems encountered by researchers in

India. **2 Hrs**

Defining the Research Problem: Research problem, selecting the problem, necessity of defining the problem, technique involved in defining a problem, an illustration. **1 Hr**

2) **Reviewing the literature:** Importance of the literature review in research, How to review the literature, searching the existing literature, reviewing the selected literature and writing about the literature reviewed. **2 Hrs**

Research Design: Meaning of research design, need for research design, features of a good design, important concepts relating to research design, different research designs, basic principles of experimental designs, important experimental designs. **3 Hrs**

3) **Measurement and Scaling:** Measurement in research, measurement scales, sources of error in measurement, scaling, meaning of scaling and important scaling techniques **2 Hrs**

Data Collection: Collection of primary data, observation method, interview method, collection of data through questionnaires, collection of data through schedules, difference between questionnaires and schedules, collection of secondary data. **2 Hrs**

4) **Testing of Hypotheses:** What is a Hypothesis? Basic concepts concerning testing of hypotheses, procedure for hypothesis testing, flow diagram for hypothesis testing, measuring the power of a hypothesis test, tests of hypotheses. **2 Hrs**

5) **Interpretation and Report Writing:** Meaning of interpretation, technique of interpretation, precaution in interpretation, significance of report writing, different steps in writing report, layout of the research report, types of reports, oral presentation and mechanics of writing a research report, precautions for writing research reports, plagiarism and its significance. **3 Hrs**

6) **Introduction to Intellectual Property Rights:** Meaning and conception of IPR, competing, rationale for protection, international conventions, world court. **1 Hr**

Copy right: Historical evolution of the law on copy right, meaning, content, substance, ownership, primary, special rights, obligations, period, assignment and relinquishment of copy rights. License and application for registration of copy right.

Patents: Meaning of Patent, purpose and policy object of patent law, gains to inventor, application of patents, joint application, discovery and invention, patentable and non-patentable inventions, publications and public use, priority date and its purpose, procedure for obtaining patent. Stages of procedure, refusal to grant patent - consequence, protection period, drafting if claims, grant of patent and significance of date of patent and date of ceiling. Services available with patent office, jurisdiction, appellate authorities, powers and

obligations of central government, patent agentand controller – not a civil court. **4 Hrs**

Industrial Design: Concepts and Significance **1 Hr**

Trademarks: Definitions and conceptions of Trademark, advantages of registration, marks which are not registrable, known and well-known trade marks, application for registration and procedure for registration, procedure and certification of Trademarks. **1 Hr**

Infringement and Remedies: Meaning of infringement, acts of infringements, suit against infringement and defence against infringement, reliefs and certificate of validity. **1 Hr**

The information Technology Act: Definitions, certifying authority, meaning of compromise of digital signature, offences and penalties, applicability of IPRs, cybercrimes, adjudicating officer, violation, damages and penalties, Cyber regulation appellate tribunal, World Wide Web and domain names and cyber flying. Self study. **1 Hr**

Reference Books:

1) C.R. Kothari, GauravGarg, Research Methodology: Methods and Techniques, New Age International, 4th Edition, 2018.

2) Ranjit Kumar,Research Methodology a step-by-step guide for beginners, SAGEPublications, 3rd Edition, 2011.

3) Fink A, Conducting Research Literature Reviews: From the Internet to Paper, SagePublications, 2009.

4) N. K. Acharya, Text book on Intellectual Property Rights,4th Edition, Asia Law House, Hyderabad.

20PMEC100	**Applied Mathematics**	**(4-0-0) 4**

Contact Hours: 52

Course Learning Objectives (CLOs): This course will enable students to: Acquaint with principles of Probability theory, Random process, Linear Algebra, Wavelet transforms Laplace transform and Linear programming problems and apply the knowledge in the applications of Electronics and Communication Engineering Sciences.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the		1,2	

	probability models arising in random processes.			
CO-2	Learn the concept of Wavelets and its Applications to Denoising**.**		1,2	
CO-3	Apply Linear Algebra, QR and singular value decomposition techniques for data compression, least square approximation in solving inconsistent linear systems.		1,2	
CO-4	Apply transform method to solve one-dimensional wave equation, one-dimensional heat equation,Laplace equation, Poisson equation.		1,2	
CO-5	Solve system of linear and non-linear equation arising in engineering fields		1,2	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	2.0	-	-	-	-

Pre-requisites: Basics of Probability, Differentiation and Integration, Vectors.

Contents:

1) **Probability Theory:** Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions example. **10 Hrs**
2) **Linear Algebra:** Groups, Fields, Binary Field Arithmetic, Construction of Galois Field and its basic properties. Vectors, matrices, Vector spaces.
   Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations**.** **12 Hrs**
3) **Introduction to Wavelets Theory:** Introduction, The origin of wavelets, wavelets and other reality transforms. Wavelets in future. Continuous Wavelets: First level of introduction of wavelet transforms. Continuous time frequency representation of signals. Discrete Wavelet Transform signal decomposition (Analysis) frequency response, signal reconstruction. Applications of Wavelets in science and Engineering.
   Denoising: Introduction, Denoising using wavelet shrinkage – statistical modelling and estimation, Noise estimation, Denoising Images with MATLAB.

10 Hrs

4) **Transform Methods:** Laplace transform methods for one dimensional wave equation–Displacement sina string–Longitudinal vibration of a elastic bar.Fourier transform methods for one dimensional heat conduction problems. Fourier transform methods for Laplace equation and Poisson equation. **10 Hrs**
5) **Linear and Nonlinear Programming:** Simplex Algorithm-Two Phase and Big M techniques-Duality theory-Dual Simplex method, Nonlinear Programming–Constrained extremal problems-Lagranges multiplier method Kuhn-Tucker conditions and solutions. **10 Hrs**

Reference Books:

1) Richard Bronson, "Schaum's Outlines ofTheory andProblems ofMatrix Operations", McGraw-Hill, 1988.
2) Venkataraman M K," Higher Engineering Mathematics", National Pub.Co,1992.
3) Sneddon,I.N., "Elements of partial differential equations", Dover Publications, 2006.
4) TahaH A, "Operations research- An Introduction", Mc Milan Publishing Co, 1982.
5) K.P. Soman, K.I. Ramachandran, Dr.G.Resmi; Insight into Wavelets (From theory to Practice), PHI Publications,3rd edition. 2010.

20PDEC100	Digital Circuits and Logic Design	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on threshold logic, fault detection and location in combinational circuits. It also covers the detailed sequential machine minimization procedures, state assignments using partitions, machine decomposition, state identification and fault detection experiments for sequential machines.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**List** elementary properties of threshold element and **logic design** of switching circuit by threshold elements	-	4,5	1
CO-2	**Explain, analyze and design of** different fault detection and fault location experiments for	4,5	3	

	combinational logic circuits and sequential machines.			
CO-3	**Analyze** different techniques of failure tolerant design		3,4	
CO-4	**Analysis and application** of algorithms for Simplification of completely and incompletely specified sequential machines.		5	2,6
CO-5	**Choose** and **adapt** techniques to decompose the sequential machine into series components, parallel components and to achieve input independency, reduction in the output dependency	4,5		2,6
CO-6	**Design** and **Implement** homing experiments, distinguishing experiments and machine identification experiments.			4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2	2	2.2	2.5	1

Pre-requisites: Boolean Algebra, Logic Design

Contents:

1) **Threshold Logic:** Introductory Concepts, Synthesis of Threshold Networks **04 Hrs**
2) **Reliable Design and Fault Diagnosis Hazards:** Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure Tolerant Design, Quadded Logic. **15 Hrs**
3) **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite - State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. **08 Hrs**
4) **Structure of Sequential Machines:** Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines.

15Hrs

5) **State-Identifications and Fault-Detection Experiments:** Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences. **10 Hrs**

Activity beyond Syllabus:

Seminar/Demonstration, Case studies on various fault detection techniques.

Reference Books:

1) ZviKohavi, "Switching and Finite Automata Theory", 2nd Edition. Tata McGraw Hill Edition.

2) Charles Roth Jr.,"Digital Circuits and logic Design", Thomas Asia Pte Ltd., Singapore, 6th Edition, 2004.

3) Parag K Lala, "Fault Tolerant And Fault Testable Hardware Design", Prentice Hall Inc. 1985

4) E. V. Krishnamurthy, "Introductory Theory of Computer", Macmillan Press Ltd, 1983.

5) Mishra &Chandrasekaran, "Theory of computer science Automata,Languages and Computation", 2nd Edition, PHI, 2004.

20PDEC101 Digital System Design using Verilog (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on design of various combinational and sequential circuits and design methodology. It also discusses the implementation of advanced digital circuits on programmable devices of varied complexity.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the basic concepts of digital system design using verilog.	-	4	-
CO-2	**Design** the real life applications using verilog.	4	5	1
CO-3	**Design** and **Model** various sequential circuits and memories using verilog.	4	5	-
CO-4	**Describe** various programmable Logic Devices.	-	5	-
CO-5	**Design** processors and controllers using Verilog, for embedded applications.	5	-	6
CO-6	**Elaborate** different I/O devices and fault modeling techniques.	-	-	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	-	2.66	2.25	1

Prerequisites: Digital Circuit Design, HDL Programming using verilog

Contents:

1) **Introduction and Methodology**: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.
   Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **12Hrs**

2) **Sequential Basics**: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology. **10 Hrs**
3) **Memories**: Concepts, Memory Types, Error Detection and Correction. **06 Hrs**
4) **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **06 Hrs**
5) **Processor Basics**: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **05 Hrs**
6) **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **08 Hrs**
7) **Design Methodology**: Design flow, Design optimization, Design for test. **05 Hrs**

Reference Books:

1) Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using Verilog", Elsevier, 2010.
2) Charles H. Roth, Jr., Lizy Kurian John, ByeongKil Lee, "Digital Systems Design Using Verilog", 1/e, Cengage Learning, 2014.
3) Samir Palnitkar, "Verilog HDL", 2/e, Pearson Education, IEEE 1364-2001Compliant, 2015.
4) Nazeih M Botros,"HDL Programming, VHDL and Verilog", Dreamtech Press, 2007.

20PDEE150 Introduction to Artificial Intelligence & Machine Learning (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on introduction to the fundamental concepts in artificial intelligence & machine learning. Topics covered include linear modeling, Bayesian approach, classification, clustering and popular machine learning algorithms in each topic. The course also discusses various issues related to the application of artificial intelligence using machine learning techniques.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Recognize** the characteristics of artificial intelligence systems that make it useful to real-world problems		3,1	2
CO-2	**Analyze** the situations of applying variety of mathematical models	3	1	

	and algorithms for machine learning			
CO-3	**Compare** and **justify** various mathematical models and algorithms used in machine learning	4,1	3	2
CO-4	**Justify** the selection of various classification and regression supervised/unsupervised learning problems of machine learning		3,1	
CO-5	**Select** and **implement** machine learning techniques that are suitable for the applications under consideration	4	3,1	
CO-6	**Evaluate** the performance of various machine learning algorithms		3	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.0	1.0	2.2	3.0	---	----

Pre-requisites: Basics of probability and statistics, Linear algebra

Contents:

1) **Introduction to Artificial Intelligence:** History of artificial intelligence, Propositional logic; basics of propositional logic, Resolution, Artificial intelligence applicatons, First order logic; basics of first order logic, certain knowledge representation; Taxonomic knowledge, Frmames, Nonmonotonic logic. **08 Hrs**
2) **Linear Modeling-A Least Squares Approach:** Linear Modeling, Making Predictions, Vector/Matrix Notation, Non-Linear Response from a Linear Model, Generalization and Over-Fitting, Regularized Least Squares. **05 Hrs**
3) **Linear Modeling-A Maximum Likelihood Approach:** Errors as Noise, Random Variables and Probability, Popular Discrete Distributions, Continuous Random Variables - Density Functions, Popular Continuous Density Functions, Likelihood, The Bias-Variance Trade-off, Effect of Noise on Parameter Estimates, Variability in Predictions. **09 Hrs**
4) **The Bayesian Approach to Machine Learning**: A Coin Game, The Exact Posterior, The Three Scenarios, Marginal Likelihoods, Hyper parameters, Graphical Models, A Bayesian Treatment of the Olympic100m Data, Marginal

Likelihood for Polynomial Model Order Selection. **09 Hrs**

5) **Bayesian Inference:** Non-Conjugate Models, Binary Responses, A Point Estimate - The Map Solution, The Laplace Approximation, Sampling Techniques. **08 Hrs**
6) **Classification:** The General Problem, Probabilistic Classifiers, Non-Probabilistic Classifiers, Assessing Classification Performance, Discriminative and Generative Classifiers. **05 Hrs**
7) **Clustering:** The General Problem, K-Means Clustering, Mixture Models. **08 Hrs**

Activity beyond Syllabus: Program development for the machine learning Algorithms in MATLAB/ Python.

Reference Books:

1) Simon Rogers, Mark Girolami, "A First Course in Machine Learning", second edition, CRC Press, 2017.
2) Richard E. Neapolitan & xia Jiang, "Artificial Intelligence with an introduction to machine learning", second edition, CRC press, 2018.
3) Ethem Alpaydin, "Introduction to Machine Learning", Prentice Hall of India, Third edition, 2014.
4) Mohssen Mohammed, Muhammad Badruddin Khan, Eihab Bashier Mohammed Bashier, "Machine Learning, Algorithms and Applications", CRC Press, 2017.
5) Michael Paluszek, Stephanie Thomas, "MATLAB Machine Learning", A press, 2017.

20PDEE151 Digital Control Systems (4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

The course focuses on digital control system from a modern and intuitive perspective. It imparts analysis and design principles of discrete-data control systems. The course deals with stability analysis of linear systems.

Course Outcomes(COs):

Description of the course outcomes: At the end of the course the students will be able to:		**Mapping to POs (1 to 6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** and Obtain the mathematical and analytical treatment of digital data and signals in control systems.	2		

CO-2	**Analyse** discrete data control systems using z-transform.	1,3	4	
CO-3	**Analyse** pulse transfer function, block diagrams and signal flow graphs.	1,3	4	
CO-4	**Evaluate** and **Analyse** the Stability of digital control systems using state-variable technique.	1,3	4	
CO-5	**Analyse** and **design** discrete data control systems using the concepts of controllability, observability and stability.	1,3	4	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3	3	3	2	-	-

Pre-requisites:
Basics of continuous data control systems, linear systems theory.

Contents:

1) **Signal Conversion and Processing:** Introduction, Digital Signals and Coding, Data Conversion and Quantization, Sample-and-Hold Devices, DAC, ADC, Mathematical Modeling of the Sampling Process, The Sampling Theorem, Mathematical Modeling of Sampling by Convolution Integral, Flat-Top Approximation of the Finite-Pulsewidth Sampling, s-Plane Properties of $F^*(s)$, Data Reconstruction and Filtering of Sampled Signals, The Zero-Order Hold, The First-Order Hold, The Polygonal Hold and the Slewer Hold. **10 Hrs**
2) **The z-Transform:** Introduction, Examples, Relationship between the s-Plane and the z-Plane, The Inverse z-Transform, Theorems, Limitations and Applications of the z-Transform, Signals between the Sampling Instants. **10 Hrs**
3) **Transfer Functions, Block Diagrams and Signal Flow Graphs:** Introduction, The Pulse Transfer Function and the z-Transfer Function, Pulse Transfer Function of the Zero-Order Hold and the relation between G(s) and G(z), Closed-Loop Systems, The Sampled Signal Flow Graph, The Modified z-Transfer Function, Multirate Discrete-Data Systems. **10 Hrs**
4) **The State-Variable Technique:** Introduction, State equations and State Transition equations of Continuous-Data systems, State equations of Discrete-Data Systems with Sample-and-Hold devices, State equations of digital systems, Digital simulation and approximation, The state transition equations, Relationship between state equations and transfer functions, Characteristic equation, Eigenvalues and Eigenvectors, Diagonalization of the **A** Matrix, Jordan

Canonical Form, Methods of Computing the state transition matrix, Relationship between state equations and High-order difference equations, Transformation to Phase-variable canonical form, The state diagram, Decomposition of Discrete-data transfer functions, State diagrams of discrete-data systems, State-variable analysis of response between sampling instants, State-variable analysis of systems with Multirate, skip-rate and non-synchronous samplings. **12 Hrs**

5) **Controllability, Observability and Stability:** Introduction, Controllability of linear time invariant discrete-data systems, Observability of linear time invariant discrete-data systems, Relationships between Controllability, Observability and Transfer functions, Controllability and Observability versus sampling period in a discrete-data system, Stability of linear digital control systems, Stability tests of discrete-data systems. **10 Hrs**

Activity beyond Syllabus:

Using MATLAB to analyse stability and behavior of discrete-data control systems.

Reference Books:

1) Benjamin C. Kuo, "Digital Control Systems", 2nd edition, Oxford University Press, 1992.
2) Katsuhiko Ogata, "Discrete-Time Control Systems", 2nd edition, Eastern economy edition, PHI, 2011.
3) M. Gopal, "Digital Control and State Variable Methods", Tata McGraw-Hill Publisher, 1997.
4) Charles L. Phillips and H. Troy Nagle, "Digital Control System Analysis and Design", 3rd edition, Pearson, 1995.
5) M. Sami Fadali and Antonio Visioli, "Digital Control Engineering Analysis and Design", 2nd edition, Elsevier, 2013.

20PDEE152 Automotive Electronics (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on fundamental principles of Electronic Engine control system, construction and operation of sensors and actuators, role of electronics in vehicle motion control, instrumentation and advanced features for safety and comfort in vehicles.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:	**Mapping to POs(1 to 6)**		
	Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**

CO-1	**Explain** various parts and operation of automobile system, electronic control system and microcomputer system.		1	6
CO-2	**Explain** and **apply** control system approach to Engine control and **define** and **analyze** various performance parameters.	3	4	
CO-3	**Describe** the construction and operation of various sensors and actuators used in automotive control applications.		3	5
CO-4	**Analyze** and **explain** vehicle motion control system and automotive instrumentation systems.	4	3	
CO-5	**Describe** various advanced electronic features, communication protocols and diagnostics		5	4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	-	2.33	2	1.5	1

Pre-requisites: Basics of Automobiles and Engine, Analog and Digital Electronic Circuits, Control systems and microcontrollers

Contents:

1) **Automotive Fundamentals:** Overview of automotive industry, Evolution of Automotive Electronics, Automotive supply chain Automobile Physical configuration, The SI Engine and its operation, Engine control, Ignition system, Ignition Timing, Diesel Engine, Hybrid vehicle configuration, Drive Train, Brakes, Suspension, Steering System, V-Model development cycle. **08 Hrs**
2) **Control System Approach:** Open loop and closed loop control systems, Proportional Controller, Proportional-Integral controller, Closed Loop Limit Cycle control. **04 Hrs**
3) **Microcomputer Systems:** Microcontroller applications in Automotive systems, Instrumentation applications of microcomputers, Microcomputers in control systems. **03 Hrs**
4) **The Basics of Electronic Engine Control:** Motivation for electronic engine control, Government Test procedures, Concept of an electronic engine control system, Definition of General Terms and Engine performance terms, Engine Mapping, Control Strategy, Electronic fuel control system, Analysis of intake manifold pressure, Idle speed control, Electronic Ignition. **10 Hrs**

5) **Sensors and Actuators:** Control system applications of sensors and actuators, Airflow rate sensors, Engine Crankshaft angular position sensors, Throttle angle sensor, Temperature Sensors, Sensors for feedback control, Knock sensors, Engine control actuators, variable valve Timing. **10 Hrs**
6) **Vehicle Motion Control:** Typical Cruise control system, Cruise control electronics, Antilock braking System, Electronic Suspension system, Electronic steering control **04 Hrs**
7) **Automotive Instrumentation:** Modern Automotive Instrumentation, Input and Output Signal Conversion, Sampling, Fuel Quantity measurement, Coolant Temperature measurement, Oil Pressure measurement, Vehicle Speed measurement. **04 Hrs**
8) **Advanced Automotive Electronic Systems:** Occupant Protection Systems, Collision avoidance RADAR warning system, Low Tyre-pressure warning system, Sensor and Control Signal Multiplexing, Navigation **05 Hrs**
9) **Communication Protocols:** CAN protocol, LIN, Flexray **04 Hrs**

Reference Books:

1) William B. Ribbens, "Understanding Automotive Electronics", 6/e, Newnes, 2003
2) A. K. Babu, " Automotive Electrical and Electronics", 2/e, Khanna publishing, 2016
3) Tom Denton, "Automobile Electrical and Electronic Systems", 5/e, Institute of Motor Industry, 2017
4) Nijamuz Zaman, "Automotive Electronics Design fundamentals", Springer, 2015

20PDEE153 Nano Electronics (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the study of various nanostructures, their properties and applications. The course also focuses on understanding the physical, chemical and fabrication aspects of nanostructures and nanodevices at nanoscale, relevant to the field of electronics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** and **appreciate** the significance of Nano electronics, as an emerging area in the field of electronics.	3	-	-
CO-2	**Identify** various nanostructures,		4	

	discuss their properties and applications			
CO-3	**Analyze** and **discuss** the physical effects occurring in various Nano devices.	4		5
CO-4	**Classify** different microscopic techniques required to study novel properties of nanostructures occurring at nano scale.		4	
CO-5	**Compare** and **differentiate** various quantum structures, self assembly techniques.			1
CO-6	**Discuss** the applications of nano structures, in relevance to the field of electronics.	3	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	3	2.3	1	1

Pre-requisites:

Physics, Electronics, Engineering Mathematics, Material Science

Contents

1) **Introduction:** Overview of nanoscience and engineering, Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale. Fabrication methods: Top down processes, Bottom up processes, methods describing the growth of nanomaterials, ordering of nanosystems. **10 Hrs**
2) **Characterization:** Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques.

   Inorganic semiconductor nanostructures: Overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states. **12 Hrs**
3) **Fabrication techniques:** Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching. Strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations,

thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

Physical processes: Modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural. **14 Hrs**

4) **Carbon Nanostructures:** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **06Hrs**
5) **Nanosensors:** Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, Nanosensors Based On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future.

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures. **10 Hrs**

Reference Books:

1) Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2) Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology” , John Wiley, Copyright 2006, Reprint 2011.
3) T Pradeep, “Nano: The essentials-Understanding Nanoscience and Nanotechnology”, TMH.
4) Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “ Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

20PDEL101 Digital Circuits Simulation Laboratory (0-0-3) 2

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on design of digital circuits and verifying the same by using LabVIEW and Verilog code. The experiments are meant to give a good understanding of tools for realization of digital systems.

Course Outcomes (COs):

Description of the course outcomes: At the end of the course the students will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Demonstrate** logic gate implementation using LabVIEW /Verilog code.		4	
CO-2	**Design** different digital circuits and verify the functional simulation by using Graphical programming tool LabVIEW.	3	5	
CO-3	**Design** a digital system for addition and multiplication.	3		
CO-4	**Implement** sequential digital circuits on FPGA board.	3	4	
CO-5	**Develop** LIFO and FIFO systems.	3	4	
CO-6	**Build** and **Implement** application based digital system as a part of Hobby Projects.	3,4	1,2,5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	3	2.25	2	1

Pre-requisites: Digital Electronics, Verilog HDL

Contents:

PART A

Graphical Programming for digital circuits using LabVIEW

1) Design of Binary Subtractors
2) Design of Encoder (8 x 3), Decoder(3 x 8)
3) Design of Multiplexer (8 x 1) and Demultiplexer (1 x 8)
4) Design of FF (SR, D, T, JK, and Master Slave with delays)
5) Design of registers using latches and flip-flops
6) Design of 8-bit Shift registers

Part B

FPGA DIGITAL DESIGN

Download the programs on FPGA/CPLD boards and performance testing may be done using pattern Chip scope pro apart from verification by simulation with any of the frontend tool.

1) Write Verilog code for the design of 8-bit.

i. Carry Ripple Adder

ii Carry Look Ahead adder

iii. Carry Skip Adder

2) Write Verilog Code for 8-bit

i. Array Multiplication

ii. Booth Multiplication (Radix-4)

3) Write Verilog code for 4/8-bit

i. Magnitude Comparator

ii. LFSR

4) Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.

5) Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg11101 (with and without overlap) any sequence can be specified.

6) Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

Reference books:

1) Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using Verilog”, Elsevier, 2010.

2) Charles H. Roth, “Fundamentals of logic design”, Thomson Learning, 2004.

3) NC Launch User Guide Product Version 3.1 June 2000

4) NC Verilog Simulator Help Product Version 3.1 June 2000

20PDEL102 Seminar (0-0-2)1

Contact Hours: 30

Course Learning Objectives (CLOs):

Seminar is to train students towards independent learning, review of technical papers, demonstrate sound knowledge of the selected topic, preparing the report and presentation of the same.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1 to 6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** technically relevant and innovative topic from refereed technical journals/conferences	1	3	
CO-2	**Understand and analyze** the selected topic.		1,4,5	
CO-3	**Compare** different techniques relevant to the selected topic.		3	

CO-4	**Organize** the topic in a systematic manner and **prepare** the report in a specific format	2	6	
CO-5	**Present** the work in a systematic way.	2	6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.5	3	2	2	2	2

II semester

20PDEC200	Digital VLSI Design	(4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on understanding the construction details and electrical characteristics of MOSFETs, designing different digital applications of MOSFETs for the high speed and low power considerations.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction and the characteristics of MOS structures.			5
CO-2	**Design** of an Inverter with different loads.		4,5	
CO-3	**Design** digital circuits using various design styles.	4,5		6
CO-4	**Discuss** Bi-CMOS gates **and Compare** the performance of CMOS and Bi-CMOS logic circuits.	4,5	6	
CO-5	**Explore** various memory structures and low power design techniques.		4,5	
CO-6	**Design** and Validate performance of digital systems.	4,5	1,3,6	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	1	2	2.6	2.6	1.6

Pre-requisites: Digital Circuit Design, Basic VLSI Design

Contents:

1) **MOS Field Effect Transistors(MOSFETs):** Device structure and physical operation, Current voltage characteristics, MOSFET circuits as DC, MOSFET as an amplifier and switch, Biasing in MOS Amplifier circuits. **08 Hrs**

2) **MOS Inverters:** Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter. MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints. **08 Hrs**

3) **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **06 Hrs**

4) **Semiconductor Memories**: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Non-volatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). **08 Hrs**

5) **Low-Power CMOS Logic Circuits:** Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits. **08 Hrs**

6) **Bi-CMOS Logic Circuits:** Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behaviour of BJTs, Basic Bi-CMOS Circuits: Static Behaviour, Switching Delay in Bi-CMOS Logic Circuits, Bi-CMOS Applications. **08 Hrs**

7) **Chip Input and Output (I/O) Circuits:** Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **06 Hrs**

Activity beyond syllabus: Design of Digital Circuits using Cadence Software.

Reference Books:

1) Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill,Third Edition,2003.
2) Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
3) Jan M.Rabaey, Massoud Pedram, “Low Power Design Methodologies” Kluwer Academic, 2010.
4) ADEL Sedra, Kenneth C Smith, "Microelectronic Circuits Theory & Applications," Oxford Publication, 2013.

20PDEC201	Advanced Embedded System Design	(4-0-0)4

Contact hours: 52

Course Learning Objectives (CLOs):

The course focuses on real time task scheduling, modifications required in multiprocessor environment, handling of resource sharing and database requirements.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** the principles and Characteristics of various applications of basic and Advanced Embedded systems.	3		1
CO-2	**Realize** different EDA tools and Embedded Firmware Design.		3,4	2
CO-3	**Program** 32-bit ARM Micro controller.	1		
CO-4	**Explain** task, thread, process and various scheduling techniques.		4	5
CO-5	**Distinguish** between Dis-assembler or Decompiler, Simulator, Emulators and Debugging		5	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	1	2.5	2	1.5	-

Pre-requisites: Operating systems

Contents:

1) **Typical Embedded System**: Core of the Embedded System, Memory,Sensors and Actuators, Communication Interface. **8 Hrs**
2) **Embedded Hardware Design and Development**: EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Net list creation, PCB Layout Design Building blocks, Component placement, PCB track routing.
   Embedded Firmware Design and Development: Embedded Firmware Design Approaches Embedded Firmware Development Languages. **14 Hrs**
3) **ARM-32 bit Microcontroller family**: Architecture of ARM Cortex-M3, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex

M3. Exceptions Programming. Advanced Programming Features, Memory Protection. Debug Architecture. **12 Hrs**

4) **Real-Time Operating System (RTOS) based Embedded System Design:** Operating System Basics, Types of OS, Comparison of different RTOS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization. **10 Hrs**
5) **The Embedded System Development Environment:** The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan. **8 Hrs**

Activity beyond Syllabus:
Case study and Implementation of RTES.

Reference Books:

1) Shibu K. V., "Introduction to Embedded Systems", Tata McGraw Hill Education Pvt. Ltd., 2009.
2) Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3",Newnes, (Elsevier),2008.
3) James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008.
4) Rajkamal "Embedded Systems architecture, programming and Design" Tata McGraw-Hill Education, second edition, 2011.

20PDEE250 Parallel Computing (4-0-0) 4

Contact hours: 52

Course Learning Objectives (CLOs):
The course focuses on basic parallel architectures and parallel algorithm design. The Message-Passing Programming (MPI) is introduced to provide an insight into various built-in functions. The shared memory programming deals with parallelization of simple looping techniques.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Identify** the need for concurrency and parallel computing.		3	

CO-2	**Realize** different parallel architectures based on instructions set architecture		3	
CO-3	**Explore** the various techniques for shared memory programming.		4	5
CO-4	**Explain** the message passing model and **explore** the built-in functions of message passing interface		4	
CO-5	**Design** parallel algorithms		4,6	5

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	-	2	2	1	2

Pre-requisites: Operating systems

Contents:

1) **Overview of Parallel Computing:** Evolution of Supercomputing, Modern Parallel Computers, Concurrency, Data Clustering, Programming Parallel Computers. **6 Hrs**
2) **Parallel Architectures:** Introduction, Interconnection Network, Processor Arrays, Multiprocessors, Centralized/ Distributed Multiprocessors, Multicomputer, Flynn's Taxonomy SISD, SIMD, MISD, MIMD. **10 Hrs**
3) **Shared Memory Programming:** Introduction, The shared memory model, Parallel for Loops, Declaring Private Variables, Critical Sections, Reductions, Performance Improvements, More General Data Parallelism, Functional Parallelism. **12 Hrs**
4) **Message Passing Programming**: Introduction, The Message-Passing Model, The Message-Passing Interface, Circuit Satisfiability, Introduction to Collective Communication, Function MPI_Reduce, Benchmarking Parallel Performance, Functions MPI_Wtime and MPI_Wtick, Function MPI_Barrier. **12 Hrs**
5) **Parallel Algorithm Design**: Introduction, The task/Channel Model, Foster's Design Methodology, Partitioning, Communication, Agglomeration, Mapping, Boundary Value Problem, Finding the maximum, The n-Body Problem, Adding Data Input. **12 Hrs**

Activity beyond Syllabus:

Case study on different parallel algorithms.

Reference Books:

1) Michael J. Quinn, "Parallel Programming in C with MPI and OpenMP", McGraw Hill Education (India) Edition 2003.

2) Peter Pacheco, "An Introduction to Parallel Programming", Morgan Kaufmann Publishers, an imprint of Elsevier 2011.
3) Shameem Akhter, Jason Roberts, "Multi-Core Programming", Intel Press, 2006.
4) Ananth Grama, Anshul Gupta, George Karypis, Vipin Kumar, "Introduction to Parallel Computing", Addison Wesley, 2003

20PDEE251 Low Power Circuits & Systems (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on basics and advanced techniques in the low power design. Describe the various power reduction and the power estimation methods and also explain power dissipation at all layers of design hierarchy. Apply State-of-the art approaches to power estimation and reduction. Practice the low power techniques using current generation design style and process technology.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	I**dentify** the sources of power dissipation in CMOS circuits.		4	
CO-2	**Perform** power analysis using simulation based and probabilistic approaches.		3	4
CO-3	**Use** optimization and trade-off techniques to reduce power dissipation of the digital circuits.	4	5	6
CO-4	**Apply** practical low power design techniques and their analysis at various levels of design abstraction in the latest design automation environments.	4	5	6
CO-5	**Build** power efficient systems using advanced techniques.	6	4,5	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	2.2	2	1.6

Pre-requisites: Digital VLSI Design

Contents:

1) **Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **06 Hrs**
2) **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **06 Hrs**
3) **Probabilistic power analysis:** Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **05 Hrs**
4) **Circuit:** Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. **05 Hrs**
5) **Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **04 Hrs**
6) **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **04 Hrs**
7) **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation. **04 Hrs**
8) **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division**.** **05 Hrs**
9) **Low power memory design:** Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM. **05 Hrs**
10) **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

    Advanced Techniques: Adiabatic computation, pass transistor logic synthesis, Asynchronous circuits. **08 Hrs**

Reference Books:

1) Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.
2) Jan M.Rabaey, Massoud Pedram, “Low Power Design Methodologies” Kluwer Academic, 2010.
3) Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000.
4) A. P. Chandrasekaran and R. W. Broadersen, “Low power digital CMOS design”, Kluwer Academic,1995.

5) A. Bellamour and M. I. Elmasri, " Low power VLSI CMOS circuit design", Kluwer Academic,1995.

20PDEE252 Digital Signal Compression (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the need for compression, various lossless and lossy compression techniques and their performance measures.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Describe** various compression techniques and **Understand** the principles of different types of quantization		4	
CO-2	**Analyze** various differential encoding methods		4	
CO-3	**Analyze** various transform coding methods	4	3,5	
CO-4	**Design** analysis / synthesis schemes for speech compression.	4	1,5	
CO-5	**Understand** various speech, image and video compression standards.		1,5	
CO-6	**Design and compare** various lossless coding methods.	4	1,5	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	-	2	2.6	2	-

Pre-requisites: Digital Signal Processing, Digital Communication, Information Theory and Coding.

Contents:

1) Introduction: Compression techniques, Modeling & coding, Distortion criteria. **03 Hrs**

2) Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization,

Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Trellis coded quantization. **10 Hrs**

3) **Differential Encoding:** Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation. **06 Hrs**
4) **Transform Coding:** Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression. **08 Hrs**
5) **Analysis/Synthesis Schemes:** Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression. **06 Hrs**
6) **Video Compression:** Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video. **07 Hrs**
7) **Lossless Coding:** Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Dictionary techniques – LZ77, LZ78, Applications of LZ78 – JBIG, JBIG2, Predictive coding – Prediction with partial match, Burrows Wheeler Transform, Applications – CALIC, JPEG-LS. **12 Hrs**

Reference Books:

1) K. Sayood, “Introduction to Data Compression," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.
2) N. Jayant and P. Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video,” Prentice Hall, USA, 1984.
3) D. Salomon, “Data Compression: The Complete Reference”, Springer, 2000.
4) Z. Li and M.S. Drew**,** “Fundamentals of Multimedia,” Pearson Education (Asia) Pvt. Ltd., 2004.

20PDEE253 Artificial Neural Networks & Deep Learning (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course offers an introduction to Artificial Neural Networks and Deep Learning. The course delve into selected topics of deep Learning, discussing recent models from both supervised and unsupervised learning. Special emphasis will be on convolutional architectures, invariance learning, back propagation and non-convex optimization. Also course covers models for various applications, how they are trained, validated and deployed in the wild.

Course Outcomes (COs):

Description of the Course Outcome:	**Mapping to PO (1 to 6)**		
At the end of the course the student will	**Level 3**	**Level 2**	**Level 1**

be able to:		Substantial	Moderate	Slight
CO-1	**Understand** the role of neural networks in engineering, artificial intelligence and learn basic neural network architecture.		6	2
CO-2	**Implement** Perception learning algorithm and Adaptive linear combiner.		3	1
CO-3	**Develop** delta learning rule of the output layer and Multilayer feed forward neural network with continuous perceptions.	3	4	1
CO-4	**Calculate** weight gradients in a feed forward neural network using back propagation algorithm.	3	4	2
CO-5	**Identify** the deep learning algorithms which are more appropriate for various types of learning tasks in various domains.		6	2,1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	1.0	2.7	2.0	---	2.0

Pre-requisites: Linear Algebra, Probability &Statistics

Contents:

1) **Introduction:** Neural Network, The human brain, Models of a neuron, Neural networks viewed as directed graphs, Feedback, Network architectures, Knowledge representation **02 Hrs**
2) **Single layer Perception:** Introduction, Pattern Recognition, Linear classifier, Simple perception, Perception learning algorithm, Modified Perception learning algorithm, Adaptive linear combiner, Continuous perception, Learning in continuous perception. Limitation of Perception. **06 Hrs**
3) **Multi-Layer Perceptron Networks**: Introduction, MLP with 2 hidden layers, Simple layer of a MLP, Delta learning rule of the output layer, Multilayer feed forward neural network with continuous perceptions, Generalized delta learning rule. **08 Hrs**
4) **Activation Functions, Gradient descent & Back propagation:** Sigmoid, ReLU, Hyperbolic Fns, Softmax, Gradient descent, Stochastic gradient descent, back propagation, Some problems with ANNs. **08 Hrs**
5) **Optimization& Regularization:** Overfitting and Capacity, Cross validation,

Feature selection, Regularization & Hyperparameters. **06Hrs**

6) **Introduction to Convolutional & Recurrent Neural Network:** Introduction to CNNs, Kernel filter, Principles behind CNNs, Multiple filters, CNN applications, Introduction to RNNs, unfolded RNNs, Seq2seq RNNs, LSTM, RRN applications. **10 Hrs**
7) **Deep Unsupervised Learning:** Encoder Decoder architecture, Auto-encoders (standard, sparse, denoising, contractive), Variational auto encoders, Adversarial generative networks,DBM. **06 Hrs**
8) **Applications of Deep Learning to NLP:** Introduction to NLP and vector space model semantics, Word vector representations: Continuous Skip-Gram model, Continuous of words model, Glove, Evaluations and applications in word similarity, analogy reasoning. **06 Hrs**

Activity beyond Syllabus: Seminar, Simulation based project.

Reference Books:

1) Simon Haykin, "Neural networks and Learning machines", 3/e, Pearson education, 2009.
2) Zurada and Jacek M, "Introduction to Artificial Neural Systems", West Publishing Company, 1992.
3) Goodfellow, I., Bengio, Y, and Courville A., "Deep learning", MIT press, 2016.
4) Bishop C.M., "Pattern Recognition & Machine learning", Springer, 2006.
5) Yegnanarayana, B., Artificial Neural Networks, PHI Learning Pvt Ltd 2009.

20PDEE254 IoT Applications (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on all the important design and implementation details of various functions possible with IoT such as use of specific sensors, computational devices and connectivity to the Internet.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the vision of IoT from a global context.	-	6	5
CO-2	**Determine** the market perspective of IoT.	-	6	5

CO-3	**Explore** the devices, gateways and data management in IoT.	-	4,6	-
CO-4	**Build** the state of art architecture in IoT.	4	5,6	1
CO-5	**Apply** the concepts of IoT to solve industrial and commercial building automation and real world design constraints.	4,5	1	2
CO-6	**Understand** the vision of IoT from a global context.	-	6	5

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.5	1	-	2.6	1.6	2

Pre-requisites: Fundamentals of computer network, wireless sensor network, communication & internet technology, web technology, information security.

Contents:

1) **IoT & WebTechnology:** The Internet of Things Today, time for convergence, towards the IoT universe, Internet of things vision, IoT strategic research and innovation directions, IoT applications, Future Internet technologies, Infrastructure, Networks and Communication, processes, Data management, Security, Privacy & Trust, device level Energy issues, IoT related standardization, Recommendations on research topics. **9 Hrs**
2) **Machine to Machine(M2M) to IoT:** Basic perspective: Introduction, some definitions, M2M value chains, IoT value chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An architectural overview–building architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. **10Hrs**
3) **IoT Architecture:** Introduction, State of the art, Architecture Reference Model-Introduction, Reference model and architecture, IoT reference Model, IoT reference architecture-Introduction, Functional view, Information view, Deployment and operational view, Other relevant architectural views. **10 Hrs**
4) **IoT Applications for Value Creations**: Introduction, IoT applications for industry: Future factory concepts, Brownfield IoT, Smart objects, Smart applications, Four aspects in your business to master IoT, Value creation from big data and serialization, IoT for retailing industry, IoT for oil and gas industry, Opinions on IoT application and value for industry, Home management, e-Health. **12 Hrs**

5) **Internet of Things Privacy, Security and Governance:** Introduction, Overview of governance, Privacy and security issues, Contribution from FP7 Projects, Security, Privacy and Trust in IoT-data-Platforms for smart cities, First steps towards a secure platform, Smart approach. Data aggregation for the IoT in smart cities security. **11Hrs**

Reference Books:

1) Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on Approach)”, 1st Edition, VPT, 2015.
2) Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications, 2013.
3) Cuno Pfister, “Getting Started with the Internet of Things,” Reilly Media, 2011.
4) Raj Kamal, "Internet of Things: architecture and design principles" McGraw Hill Education(India), 2017.

20PDEE255 Coding Theory (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on various error detection and error correction coding techniques in wireless communication systems.

Course Outcomes:

Description of the Course Outcome: At the end of the course the student willbe able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Apply** and **calculate** Galois field arithmetic for error control coding techniques in digital communication and data storage systems.	-	1	-
CO-2	**Design** and **analyze** Linear block codes.	4	-	5
CO-3	**Design** and **analyze** cyclic codes.	4	-	5
CO-4	**Explain** and **analyze** BCH codes, MLD codes.	-	1,2	6
CO-5	**Explain** Convolutional codes and **Analyze** decoding algorithms.	-	4,5	-
CO-6	**Explain** Concatenated Codes & Turbo Codes.	-	4,5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	-	2.5	1.5	1

Pre-requisites: Information theory & coding, Digital communication

Course Contents:

1) **Introduction to Algebra**: Construction of Galois Field GF (2m) and its basic properties, Computation using Galois Field GF (2m) Arithmetic. **04 Hrs**
2) **Linear Block Codes:** Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Hamming Codes, Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes. **08 Hrs**

3) **Cyclic Codes:** Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes – Encoding using Feedback shift register circuits, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, The (23, 12) Golay code, Shortened cyclic codes.**10Hrs**
4) **BCH Codes and Majority Logic Decodable Codes:** Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Reed – Solomon Codes, One – Step Majority logic decoding, one – step Majority logic decodable Codes, Two – step Majority logic decoding. **12 Hrs**
5) **Convolution Codes:** Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Stack and Fano sequential decoding Algorithms. **10 Hrs**
6) **Concatenated Codes & Turbo Codes:** Single level Concatenated codes, Multilevel Concatenated codes, s, Introduction to Turbo coding and their distance properties, Design of Turbo codes. **08 Hrs**

Activity beyond Syllabus: Assignments on the design of various coding techniques.

Reference Books:

1) Shu Lin & Daniel J. Costello, Jr. “Error Control Coding”, Pearson / Prentice Hall, Second Edition, 2004.
2) Blahut, R.E., “Theory and Practice of Error Control Codes”, Addison Wesley, 1984.
3) Satyanarayana P.S., “Concepts of Information Theory & coding”, Dynaram Publications, Bangalore, 2005.
4) Ranjan Bose, “Information Theory, Coding and Cryptography”, Tata McGraw-Hill Publication, 2002, ISBN: 0-07-048297-7

20PDEE256	Advanced Mobile Networks	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on existing Telecommunication networks, past wireless Communication and mobile networks, future LTE and 4G technology and brief overview of upcoming 5G technology.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1 to 6)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO 1	**Discuss** the evolution and history of wireless technology and **compare** different mobile Networks along with their common system components and channel types.	-	2,3,4	1,5,6
CO 2	**Analyze** CDMA techniques with their channel structures and **scrutinize** its operations	-	2,3,4	1,5,6
CO 3	**Understand** the basics of LTE standardization phases and specifications and **Explain** the system architecture of LTE	-	2,3,4	1,5,6
CO 4	**Analyze** the role of LTE radio interface protocols to set up, reconfigure and release the Radio Bearer, for transferring the EPS bearer.	-	2,3,4	1,5,6
CO 5	**Discuss** 4G-LTE cellular technology, architecture and features in detail.	-	2,3,4	1,5,6
CO 6	**Explain** 5G requirements, Regulations, Spectrum Analysis and Sharing for 5G spectrum. Channel modeling.	-	2,3,4	1,5,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2	2	2	1	1

Pre-requisites: Wireless Communication

Contents:

1) **Introduction to Wireless Communication and mobile networks :**Existing Telecommunication infrastructure, AMPS Systems and its Frequency plan, The Cellular concept and its analysis, Capacity improvement in cellular systems, Co

channel interference reduction.GSM and its Chanel concepts, GSM Network concept. **06 Hrs**

2) **CDMA:** Introduction to CDMA, Walsh codes, Variable tree OVSF, PN Sequences, Multipath diversity, RAKE Receiver, CDMA Receiver Synchronization. OFDM: Introduction to OFDM, Multicarrier Modulation and Cyclic Prefix, Channel model and SNR performance, OFDM Issues – PAPR, Frequency and Timing Offset Issues. **10 Hrs**
3) **LTE (Long Term Evolution) :**Introduction Overview of IP Convergence in the

mobile networks, Introduction to LTE (Long Term Evolution) and SAE/e PC/EPS,LTE Network Architecture, LTE RAN, Self-Organizing Networks (SON). **10 Hrs**
4) **LTE Interfaces and protocols** : Introduction , Interfaces and protocol types, LTE Packet Core (SAE/EPC and EPS), Evolved Packet Core (EPC) Architecture, Interfaces and Protocols, LTE-Advanced (R10 and beyond), IMS and Voice over IMS for LTE-EPC Voice over LTE Voice over LTE (VolTE), SMS over LTE. **10 Hrs**
5) **4G LTE Cellular Technology:** Network Architecture and Mobile Standards, Introduction, fourth (4^{th}) generation mobile communication, Need and scope for 4G technology, Network architecture of 4G, Geographical Coverage of 4G, Wireless LAN Integration in 4G,features of 4G technology. **06 Hrs**
6) **Overview of 5G Broadband Wireless Communications:** Evaluation of mobile technologies 1G to 4G (LTE, LTEA, LTEA Pro) , An Overview of 5G requirements, Regulations for 5G,Spectrum Analysis and Sharing for 5G. The 5G wireless Propagation Channels: Channel modeling requirements, propagation scenarios and challenges in the 5G modeling, Channel Models for Millimeter (mm) Wave MIMO Systems. **10 Hrs**

Reference Books:

1) Gary J Mullet, Introduction to Wireless Telecommunications systems and Networks, India edition, Cenage leraning 2006.
2) Arunabha Ghosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Fundamentals of LTE, Prentice Hall, Communications Engineering and Emerging Technologies.
3) Rakesh Kumar Singh, Ranjan Singh, 4G LTE Cellular Technology: Network Architecture and Mobile standards, Research article, International Journal of Emerging Research in Management & Technology, ISSN: 2278-9359 (Volume-5 Issue-12), December 2016.
4) Afif Osseiran, Jose F. Monserrat, Patrick Marsch, 5G Mobile and Wireless

Communications Technology, First edition, Cambridge University Press, 2016

20PDEE257	Software Defined Radio	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on SDR concepts, architecture and design issues in the design of transmitter and receiver in SDR. The course also covers some examples of SDR and applications of SDR.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the architecture of SDR and **quantify** the dynamic performance of SDR.	3	4	
CO-2	**Acquire** the knowledge of various SDRs and **compare** them.	4	2	5
CO-3	**Model** transmitter / receiver synchronization requirements and **measure** the errors involved.	4		
CO-4	**Differentiate** the design and implementation issues in multicarrier Modulation in comparison with single carrier and **solve** the design issues.	5	1,2	6
CO-5	**Employ** SDRs in advanced applications.		5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	3	2.7	2	1

Pre-requisites: Digital Signal Processing, Communication Systems

Contents:

1) **Introduction to Software Defined Radio:** A brief idea of Software-Defined Radio, Networking and SDR, RF architectures for SDR, Processing architectures for SDR, Software Environments for SDR, Signal Metrics and Visualization, Receive Techniques for SDR, Digital Signal Processing techniques for SDR, Transmit Techniques for SDR. **10 Hrs**
2) **Understanding SDR Hardware:** Components of a Communication System, Components of an SDR, AD9363 Details, Zynq Details, Linux Industrial Input/Output Details, Radio I/O Basics, Continuous Transmit, Latency and Data Delays, Receive Spectrum, Automatic Gain Control, Common Issues, Example: Loopback with Real Data, Noise Figure. **10 Hrs**
3) **Synchronization:** Timing Synchronization, Matched Filtering, Timing Error, Symbol Timing Compensation, Alternative Error Detectors and System Requirements, Putting the Pieces Together, Carrier Synchronization, Carrier Offsets, Frequency Offset Compensation, Phase Ambiguity, Frame Synchronization and channel Coding, Putting the Pieces Together. **12 Hrs**
4) **Channel Estimation and Equalization and OFDM:** Channel Estimation, Equalizers, Receiver Realization, Rationale for MCM: Dispersive Channel Environments, General OFDM Model, Common OFDM Waveform Structure, Packet Detection, CFO Estimation, Symbol Timing Estimation, Equalization, Bit and Power Allocation. **12 Hrs**
5) **Applications for Software-Defined Radio:** Cognitive Radio, Bumblebee Behavioral Model, reinforcement Learning, Vehicular Networking. **08 Hrs**

Reference Books:

1) Software Defined Radio for Engineers, Travis F. Collins, Robin Getz, Di Pu, Alexander M, Wyglinski, Library of Congress Cataloging-in-Publication Data, 2018.
2) P. Kenington, “RF and Baseband Techniques for Software Defined Radio,” Artech House, 2005.
3) Jeffrey Hugh Reed, “Software Radio: A Modern Approach to Radio Engineering,” Prentice Hall Professional, 2002.
4) Tony J Rouphael, “RF and DSP for SDR,” Elsevier Newnes Press, 2008.

20PDEL201	VLSI and Embedded Systems Laboratory	(0-0-3) 2

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on the design and implementation of various Digital circuits using Cadence software and different applications of embedded systems using NXP LPC1768.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design, Implement and characterize** Combinational Circuits.		3	4,5
CO-2	**Design, Implement and characterize** Sequential circuits.	3,5	4	6
CO-3	**Demonstrate** programming skills using Assembly Level Language and High-Level Language such as C		4	3
CO-4	**Explore** Interrupt Service Routine (ISR) for various sources of interrupts.		4,5	6
CO-5	**Demonstrate** the usage and importance of Inter Process Communication (IPC)	3	4,5	6

POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Mapping Level	-	-	2.25	1.8	2	1

Contents:

Part A:

Draw the Schematic and Layout for the following digital and analog circuits mentioned below with the help of Cadence tool frame work and verify the following.

a. Schematic: i) DC Analysis ii) Transient Analysis iii) Parametric analysis

b. Layout: i) DRC ii) LVS iii) RCX

1) Design CMOS Inverter with given specifications.
2) Design 2-bit full adder using half adders (Half adder has to be designed using Transmission Gates.
3) Design 4 bit UP/Down counter.

Part B:

Implement the following experiments on ARM Cortex-M3.

1) Write an Assembly language program to calculate 10+9+8+…+1
2) Write an Assembly language program to link multiple object files and link them together.
3) Write an Assembly language program to store data in RAM.
4) Write C program to output “Hello World” message using UART.
5) Write C program to design a stopwatch using interrupts.

Reference books:

1) Sung Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, 3/e, McGraw-Hill, 2008.
2) Donald D Givone, “Digital Principles and Design”. Tata McGraw Hill Edn, 2003.
3) C harles H. Roth, “Fundamentals of logic design”, Thomson Learning, 2004.
4) Joseph Yiu, “The Definative Guide to ARM Cortex-M3”, Newenes Publication.

20PDEL202 Seminar (0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

Students are provided with a platform for studying technical papers, analyze the references and compare different existing techniques found during the review of technical journals or conference proceedings. It also gives scope to perform case study or simulation of the assigned task.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Explore** the reputed journal papers in the area of interest and identify technically relevant and innovative ideas.	1	6	
CO-2	**Understand** the content of technical references and **summarize** the same.	1	3	
CO-3	**Compare** different existing techniques found in the review, perform case study or simulate the assigned work.		3, 4, 6	5

CO-4	**Organize** the outcome of the work carried out in the form of a report	2		
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	3	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	2	2	1	2