Academic Program: PG

Academic Year 2019-20

Syllabus

III & IV Semester M. Tech

Digital Electronics

Department of Electronics and Communication Engineering

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution recognized by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for 3 & 4 semester of PG (Digital Electronics) program in Electronics and Communication Engineering is recommended by Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering &Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2019-20 till further revision.

Principal Dean (Academic Program) Chairman BOS & HOD

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College Vision and Mission

Vision:

To develop competent professionals with human values.

Mission:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department Vision and Mission

Vision:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

Mission:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Programme Educational Objectives (PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Design economical, socially relevant and technically sound digital systems based on the principles of Digital Electronics.

PO5: Integrate hardware-software and apply programming practices to realize the solutions in electronics domain.

PO6: Acquire professional and intellectual integrity, ability to conceptualize, solve engineering problems with adherence to professional code of conduct and contribute to sustainable development of society at large.

Scheme for III Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration In hours
18PDEC35X	Internship***/Elective-VI	4-0-0	4	50	100	3		
18PDEE35X	Internship***/Elective VII	4-0-0	4	50	100	3		
18PDEE35X	Internship***/Elective VIII	4-0-0	4	50	100	3		
18PDEP300	Project Phase-I**	0-0-10	8	50		.	50	3
Total		**12-0-10**	**20**	**200**	**300**		**30**	

Elective VI to VIII

18PDEE350	Advances in VLSI Design	4-0-0	4	50	100	3
18PDEE351	Advanced Computer Architecture	4-0-0	4	50	100	3
18PDEE352	Artificial Neural Networks	4-0-0	4	50	100	3
18PDEE353	Cryptographic Systems	4-0-0	4	50	100	3
18PDEE354	VLSI Digital Signal Processing	4-0-0	4	50	100	3
18PDEE355	IC Fabrication Technology	4-0-0	4	50	100	3
18PDEE356	Speech Processing	4-0-0	4	50	100	3
18PDEE357	Wireless Sensor Networks	4-0-0	4	50	100	3

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorial **P**: Practical

*SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

** **Project phase-I:** The students are expected to formulate the problem and carry out the intensive literature survey along with preliminary investigations supporting the project phase-II in IV semester.

*** **Internship:** should be from the reputed industries. Duration of internship is about 4 weeks during 2nd to 3rd semester break period. Students who undergo Internship are to be exempted for one elective course in III semester.

Scheme for IV Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration In hours
18PDEP400	Project phase-II	0-0-20	22	100			100	3
Total		**0-0-20**	**22**	**100**			**100**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorial **P**: Practical

** Project phase-II: The students are expected to work on the project for the full semester in the institute/ in an industry / in reputed organization with recognized R&D center

Total Credits offered for the Second year: 42

Total Credits offered for the course: 46+42=88

III Semester

18PDEE350	Advances in VLSI Design	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

The course focuses on the theory and design principles of VLSI devices and circuits. The course concentrates on the study and analysis of various combinational and sequential MOS logic circuits for VLSI applications.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Explain** the theory, construction and the characteristics of various FET structures			3
CO-2	**Describe** the processes involved in the CMOS technology.		3,6	
CO-3	**Discuss** the basic circuits concepts involved in the design of CMOS circuits.	3,6		
CO-4	**Discuss** the various rules involved in the schematic and layout design of digital VLSI circuits.	3,5,6		
CO-5	**Explain** CMOS circuits with respect to different technologies.		3,6	
CO-6	**Identify and describe** the challenges involved in digital CMOS VLSI design.		3,5,6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	-	2.1	-	1	2.4

Pre-requisites:

Analog Electronics, Network Analysis, Digital Circuits

Course Contents:

1. **Review of MOS Circuits:** MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS. **6 Hrs.**
2. **MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS. **6 Hrs.**
3. **MIS Structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. **6 Hrs.**
5. **Beyond CMOS:** Evolutionary advances beyond CMOS, carbon Nanotubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing **6 Hrs.**
6. **Super Buffers, Bi-CMOS and Steering Logic:** Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks –NMOS and CMOS functional blocks. **8 Hrs.**
7. **Special Circuit Layouts and Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module layout. **6 Hrs.**
8. **System Design:** CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom design. **8 Hrs.**

Activity beyond Syllabus:

Mini Projects using Cadence Tool.

Reference Books:

1. Kevin F. Brennan, “Introduction to Semiconductor Device”, Cambridge publications.
2. Eugene D. Fabricius, “Introduction to VLSI Design”, McGraw-Hill International publications.
3. D. A. Pucknell, “Basic VLSI Design”, PHI Publication.
4. Wayne Wolf, “Modern VLSI Design” Pearson Education, Second Edition , 2002

18PDEE351	Advanced Computer Architecture	(4-0-0) 3

Contact Hours: 52

Course Learning Objectives(CLOs):

The course deals with the understanding quantitative principles guiding the computer system design. It focuses on enhancing the performance by addressing parallelism at different levels such as Instruction, thread, task, job. Evaluates memory hierarchy, speculations, ISA, ALU architectures, choice of I/O is major motivation.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** and **analyze** Performance; Quantitative Principles of computer design(understand and evaluate)	1,2		

CO-2	**Identify and address** concepts and challenges of ILP	1, 2	3	4
CO-3	**Investigate** Hardware and Software for VLIW and EPIC		1,2,3	5
CO-4	**Design** and **evaluating** an I/O system	1,3		5
CO-5	**Comprehend** Critical Performance Issue and **deduce** Characteristics of Scientific Applications	2	4,6	
CO-6	**Analyze** and Choose/utilise Computer Arithmetic units.		3,4	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.75	2.75	1.75	1.67	1	2

Pre-requisites:

Knowledge of Processor/Controllers, Languages-Compilers is appreciated.

Course Contents:

1. **Introduction and Review of Fundamentals of Computer Design:** **4 Hrs**
   Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design; Performance and Price-Performance; Fallacies and pitfalls; Case studies.
2. **Some topics in Pipelining:** Instruction –Level Parallelism, Its Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; **12 Hrs**

Basic concepts and challenges of ILP; Case study of Pentium 4, Fallacies and pitfalls.

3. **Introduction to limits in ILP**: Performance and efficiency in advanced multiple-issue processors. **4 Hrs.**
4. **Memory Hierarchy Design, Storage Systems:** Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies. Introduction to Storage Systems; Advanced topics in disk storage. Definition and examples of real faults and failures **8 Hrs.**
5. **I/O performance**, reliability measures, and benchmarks; Queuing theory; Crosscutting issues; Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls **6 Hrs.**
6. **Hardware and Software for VLIW and EPIC Introduction**: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism, Hardware Support for Exposing Parallelism: Predicated Instructions, Hardware Support for Compiler Speculation, The Intel IA-64 Architecture and Itanium Processor, Concluding Remarks. **6 Hrs.**
7. **Large-Scale Multiprocessors and Scientific Applications** Introduction, Inter-processor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications, Implementing Cache Coherence, The Custom Cluster Approach: Blue Gene/L, Concluding Remarks. **6 Hrs.**
8. **Computer Arithmetic**: Introduction, Basic Techniques of Integer **6 Hrs.**

Arithmetic, Floating Point, Floating-Point Multiplication, Floating-Point Addition, Division and Remainder, More on Floating-Point Arithmetic, Speeding Up Integer Addition, Speeding Up Integer Multiplication and Division, Fallacies and Pitfalls.

Reference Books:

1. Hennessey and Patterson, “Computer Architecture A Quantitative Approach”, 4th Edition, Elsevier, 2007.
2. Kai Hwang, “Advanced Computer Architecture - Parallelism, Scalability, Programmability”, 2nd Edition

18PDEE352	Artificial Neural Networks	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs)

The course focuses on both the classical and the new techniques of neural networks in supervised, unsupervised and reinforcement learning schemes. Particularly, a single perceptron and neurons, feed-forward neural networks, Kohonen's maps, associative memories, Hopfield's and many other recurrent networks will be considered.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to Pos (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** the role of neural networks in engineering, artificial intelligence and **Learn** basic neural network architecture.	6		
CO-2	**Understand** the differences		2	

	between networks for supervised and unsupervised learning.			
CO-3	**Design** single and multi-layer feed-forward neural networks.	3		
CO-4	**Develop** and train radial-basis function networks.		4	
CO-5	**Design** support vector machines.		4	
CO-6	**Analyze** principal component analysis and **Apply** Self Organizing Maps to image coding.		2	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	2	3	2	-	3

Pre-requisites:

Linear Algebra, Probability

Course Contents:

1. **Introduction:** Neural Network, The human brain, Models of a neuron, Neural networks viewed as directed graphs, Feedback, Network architectures, Knowledge representation, Learning processes, Learning tasks. **03 Hrs.**
2. **Rosenblatt's Perceptron**: Perceptron, The perceptron convergence theorem, Relation between the perceptron and Bayes classifier for a Gaussian environment, Computer experiment: pattern classification, The batch perceptron algorithm. **04 Hrs.**
3. **The Least-Mean-Square Algorithm**: Filtering structure of the LMS algorithm, Unconstrained optimization: a review, The wiener filter, The **06 Hrs**.

Least-Mean-Square algorithm, Markov model portraying the deviation of the LMS algorithm from the Wiener filter, The Langevin equation: characterization of Brownian motion, Kushner's direct-averaging method, Statistical LMS learning theory for small learning-rate parameter, Computer experiment I: Linear prediction, Computer experiment II: Pattern classification, Virtues and limitations of the LMS algorithm, Learning-rate annealing schedules.

4. **Multilayer Perceptrons**: Preliminaries, Batch learning and on-line learning, The back-propagation algorithm, XOR problem, Heuristics for making the back-propagation algorithm perform better, Computer experiment: Pattern classification, Back propagation and differentiation, The Hessian and its role in on-line learning, Optimal annealing and adaptive control of the learning rate, Generalization, Approximations of functions, Cross-validation, Complexity regularization and network pruning, Virtues and Limitations of Back-propagation learning, Supervised learning viewed as an optimization problem, Convolutional networks, Nonlinear filtering, Small-scale versus large-scale learning problems. **12 Hrs.**

5. **Kernel Methods and Radial-Basis Function Networks**: Cover's theorem on the separability of patterns, The interpolation problem, Radial-basis-function networks, K-means clustering, Recursive least-squares estimation of the weight vector, Hybrid learning procedure for RBF networks, Computer experiment: pattern classification, Interpretations of the Gaussian hidden units, Kernel regression and its relation to RBF networks. **10 Hrs.**

6. **Support Vector Machines:** Optimal hyperplane for linearly separable patterns, Optimal hyperplane for nonseparable patterns, The support vector machine viewed as a Kernel machine, Design of support vector **05 Hrs**.

machines, XOR problem, Computer experiment: pattern classification, Regression: robustness considerations, Optimal solution of the linear regression problem, The representer theorem and related issues.

7. **Principal-Components Analysis:** Principles of self-organization, Self-organized feature analysis, Principal-Components Analysis: perturbation theory, Hebbian-based maximum Eigenfilter, Hebbian-based Principal-Components Analysis, Case study: Image coding, Kernel Principal-Components Analysis, Basic issues involved in the coding of natural images, Kernel Hebbian algorithm. **06 Hrs**.

8. **Self-Organizing Maps:** Two basic feature-mapping models, Self-organizing map, Properties of the feature map, Computer experiment I: Disentangling lattice dynamics using SOM, Contextual maps, Hierarchical vector quantization, Kernel self-organizing map, Computer experiment II: Disentangling lattice dynamics using Kernel SOM, Relationship between Kernel SOM and Kullback-Leibler divergence. **06 Hrs**.

Reference Books:

1. Simon Haykin, “Neural Networks and Learning Machines” (3rd Edition), Pearson Education, 2009.
2. R. P. Lippmann, “An Introduction to Computing with Neural Nets”, IEEE ASSP Magazine, PP: 4-22, 1987.
3. Robert J. Schalkoff, “Artificial Neural Networks", McGraw-Hill, 1997.
4. Laurene Fausett, “Fundamentals of Neural Networks-Architectures, Algorithms and Applications”, Pearson Education, 2004.
5. B. Yegnanarayana, “Artificial Neural Networks”, Prentice Hall, 2006.
6. S. N. Sivanandam, S. Sumathi, S. N. Deepa “Introduction to Neural Networks using MATLAB 6.0", McGraw-Hill, 2007.

18PDEE353	Cryptographic Systems	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

Cryptographic Systems is an elective theory course at III semester PG level. Knowledge of Finite Fields and communication networks are required as a prerequisite. The course focuses on security principles, architecture, services and encryption / decryption techniques.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Analyze** and **Apply** different symmetric cryptographic techniques to encrypt and decrypt data.		3	
CO-2	**Describe** basic mathematical concepts and pseudorandom number generators required for cryptography	3,4		
CO-3	**Apply** and **estimate** different asymmetric cryptographic algorithms.	4	6	
CO-4	**Explain** authentication functions, Hash functions and MAC to authenticate and protect the encrypted data.		2	
CO-5	**Analyze** key exchange algorithms.		3	2
CO-6	**Discuss** algorithms for digital signature schemes.		3	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	1.5	2.25	3	-	2

Pre-requisites:

Communication networks and finite fields.

Course Contents:

1	**Symmetric Block Ciphers**: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6), Traditional Block Cipher structure, Data encryption standard (DES), Double DES, 3DES, The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, 2.3,2.4,Chapter 4)	**10 Hrs.**
2	**Number Theory**: Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithms. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5)	**8 Hrs.**
3	**Principles of Public-Key Cryptosystems**: The RSA algorithm, Diffie - Hellman Key Exchange, Elgamal cryptographic system, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9)	**10 Hrs.**
4	**Pseudo-Random-Sequence Generators and Stream Ciphers:** Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, NANOTEQ, RAMBUTAN, Additive generators, GIFFORD, Algorithm M, PKZIP (Text 2: Chapter 16)	**10 Hrs.**

5	**One-Way Hash Functions:** Background, SNEFRU, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14)	**8 Hrs.**
6	**Digital Signatures:** Digital signatures, Elgamal Digital Signature Scheme, Digital signature Algorithm, RSA digital signatures, Elliptic Curve DSA. (Text 1: Chapter 12: Section 12.1, 12.2, 12.4,12.5)	**6 Hrs.**

Activity beyond Syllabus:

Simulation of cryptographic algorithms.

Reference Books:

1. William Stallings, “Cryptography and Network Security Principles and Practice”, Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3.
2. Bruce Schneier, “Applied Cryptography Protocols, Algorithms, and Source code in C”, Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
3. Behrouz A. Forouzan, “Cryptography and Network Security”, 2nd Edition, TMH, 2007.
4. Atul Kahate, “Cryptography and Network Security”, 3rd Edition, TMH, 2013.

18PDEE354	VLSI Digital Signal Processing	(4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

The subject focuses on DSP Architecture, parallel processing issues in analyzing DSP Computation systems. The next part covers further the Systolic Architecture Design and pipe lined and parallel recursive and Adaptive filters.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to Pos (1-6)		
		Level 3 Substantial	Level 2 Moderate	Level 1 Slight
CO-1	**Identify** the typical signal processing tasks	3		
CO-2	**Gain knowledge** possibility of reducing the computational complexity	3	6	
CO-3	**Acquire knowledge** various architectures	2		
CO-4	**Acquire knowledge** about optimization in view of power, area and speed	2, 4		
CO-5	**Acquire knowledge** about algorithms available for the purpose of optimization	1, 4, 6		
CO-6	**Compare** the techniques / architectures	6		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3	3	3	3	-	2.5

Pre-requisites:

Knowledge of Digital Signal Processing, Analog and digital electronics, CMOS VLSI design.

Course Contents:

1	**Introduction to DSP Systems**: Introduction to DSP Systems, Iteration bound, Data Flow graphs (DFGs) representation, Loop Bound, Iteration rate, Critical loop, Critical path, Area-Speed-Power trade-offs, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power.	**10 Hrs.**
2	**Algorithmic Transformations**: Retiming Definitions and properties, Retiming Techniques, Clock period minimization, Unfolding, An algorithm for unfolding, Critical path, Applications of unfolding, Sample period reduction, Folding, Folding order, Folding Factor, register minimization techniques, register minimization in folded architecture, Forward Backward Register Allocation technique, folding of multi-rate systems, Folding Bi-quad filters, Retiming for folding.	**12 Hrs.**
3	**Systolic Architecture Design and Fast Convolution:** Introduction, system array design methodology, FIR systolic arrays, , Systolic Design for space representations containing delays Systolic architecture design methodology, Design examples of systolic architectures, selection of scheduling vector, matrix-matrix multiplication and 2-D systolic array design, Hardware Utilization efficiency, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of fast convolution algorithm by inspection.	**12 Hrs.**
4	**Algorithm Strength Reduction in filter:**Introduction, Parallel FIR filters, Polyphase decomposition, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for	**10 Hrs.**

Rank Order filters.

5	**Pipelined and Parallel Recursive and Adaptive Filters**: Introduction, pipelining in 1st order IIR digital filters, pipelining in higher order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low power IIR Filter Design using pipelining and parallel processing, pipelined adaptive digital filters.	**08 Hrs.**

References Books:

1. Parhi, K.K., "VLSI Digital Signal Processing Systems: Design andImplementation", John Wiley 2007.
2. Oppenheim, A.V. and Schafer, R.W., "Discrete-Time Signal Processing", Prentice Hall, 2009, 2nd edition.
3. Mitra, S.K., Digital Signal Processing. A Computer Based Approach, McGraw Hill, 2007, 3rd edition.
4. Wanhammar, L., DSP Integrated Circuits, Academic Press, 1999, 2005, ISBN: 978-0131543188

18PDEE355	IC Fabrication Technology	(4 - 0 - 0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

IC Fabrication Technology is an elective course at postgraduate III semester level. The course focuses on understanding of crystal growth, wafer preparation, different VLSI techniques like epitaxy, lithography, ion implementation and their comparison of performances.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Discuss** about crystal growth and wafer preparation.	1	-	4
CO-2	**Explain** epitaxy and lithography techniques.	-	1	3
CO-3	**Discuss** reactive Plasma Etching	-	1	3
CO-4	**Compare** dielectric and Polysilicon Film Deposition methods.	3	-	-
CO-5	**Analyze** ion implantation methods.	-	1	1
CO-6	**Discuss** and **Analyze** VLSI Process Integration.	-	1	3

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping level	2	-	1.5	1	-	-

Pre-requisites:

Solid state devices, Analog and Digital VLSI.

Reference Books:

1. S. M. Sze, “VLSI Technology”, McGraw-Hill, Second Edition.
2. S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc., New York, 1994, Second Edition.

18PDEE356	Speech Processing	(4 - 0 - 0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

Speech Processing course focuses on classification of speech sounds, mathematical models for speech production mechanism, various speech processing techniques in time and frequency domains. It also deals with various speech processing applications.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** the characteristics of speech signal and **classify** speech sounds		3	
CO-2	**Develop** mathematical models for speech production mechanism	3, 6		
CO-3	**Analyze** speech signal in time and frequency domain	2		
CO-4	**Explain** various feature extraction methods of speech signal	2		3
CO-5	**Differentiate** between various techniques of feature extraction and make a **comparative** study	4	3	
CO-6	**Discuss** applications of speech signal processing		2	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	-	2.6	2	3	-	3

Pre-requisites:

Digital Signal Processing

Course Contents:

1. **Production and Classification of Speech Sounds:** Introduction, mechanism of speech production, Acoustic phonetics: vowels, diphthongs, semivowels, nasals, fricatives, stop and affricates, Digital Models for Speech Sounds. **7 Hrs.**
2. **Time-domain Methods for Speech Processing:** Time dependent processing of speech, short-time energy and average magnitude, short-time average zero crossing rate. Speech vs. silence detection, pitch period estimation using parallel processing approach, short-time autocorrelation function, Pitch period estimation using autocorrelation. **7 Hrs.**
3. **Frequency Domain Methods for Speech Processing:** Introduction, definitions and properties, Fourier transforms interpretation and linear filter interpretation, sampling rates in time and frequency, Filter Bank Summation and Overlap Add methods for short-time synthesis of speech, Spectrographic displays, Pitch detection. **8 Hrs.**
4. **Linear Predictive Coding of Speech**: Basic principles of linear predictive analysis, computation of the gain of the model, Solution of LPC equations, Prediction error signal, Frequency domain interpretation of Linear Predictive Analysis, Relationship between various speech parameters, Synthesis of speech from linear predictive parameters, Applications of LPC parameters. **8 Hrs.**
5. **Homomorphic Speech Processing:** Introduction, homomorphic

systems for convolution, the complex cepstrum of speech, Pitch detection, Formant estimation, homomorphicvocoder. **7 Hrs.**

6. **Speech Synthesis:** Principle, Synthesis Based on Waveform Coding, Synthesis Based on Analysis-synthesis Method, Synthesis Based on Speech Production Mechanism, Synthesis by Rule, Text-to-speech Conversion. **7 Hrs.**
7. **Speech Recognition:** Principles of Speech Recognition, Speech Period Detection, Spectral Distance Measures, Structure of Word Recognition System, Dynamic time Warping, Hidden Markov Model. **8 Hrs.**

Activity beyond Syllabus:

MATLAB simulation of theoretical concepts.

Reference Books:

1. L. R. Rabiner and R. W. Schafer, “Digital Processing of Speech Signals", Pearson Education (Asia), 2004.
2. SadaokiFurui, “Digital Speech Processing, Synthesis and Recognition”, Marcel Dekker, INC
3. Lawrence Rabinar and B. Juang, “Fundamentals of Speech Recognition”, Pearson Education, 2003.
4. T. F. Quatieri, “Discrete Time Speech Signal Processing”**,** Pearson Education Asia, 2004.

18PDEE357	**Wireless Sensor Networks**	**(4-0-0) 4**

Contact Hours: 52

Course Learning Objectives(CLOs):

The course focuses on basic Wireless Sensor Network technology and supporting protocols with emphasis placed on standardization of basic sensor systems. This

course also provides a survey of sensor technology, medium access control protocols and address physical layer issues. The other part of the course discusses key routing protocols for sensor networks, design issues, sensor management, sensor network middleware, and operating systems.

Course Outcomes (COs):

Description of the Outcome: Upon completion of the course, the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Explain** the background, overview and architectural elements of wireless sensor networks.		1,2	
CO-2	**Apply** knowledge of wireless sensor networks(WSN) to various application areas.	3,4	1,2,5	
CO-3	**Outline**the basics of wireless sensor technology	5	1,2	
CO-4	**Discuss &Analyse** the MAC, Transport, Routing protocols for wireless sensor networks.	6		
CO-5	**Estimate** all points related to the Middleware for Wireless Sensor Networks,	1,2,3,4		
CO-6	**Identify** and **observe** issues related to Network management, Network operating systems for Wireless Sensor Networks	1,2,3,4		
CO-7	**Illustrate** Network Operating	4,5		

	Systems for Wireless Sensor Networks.			
CO-8	**Conduct** performance analysis of WSN and manage WSN.	5,6		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	1.5	2	2.5	3

Pre-requisites:

Basic of Computer communication networks, Basics of wireless networks.

18PDEP300 Project Phase - I (0-0-15) 8

Contact Hours:120

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote team work. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** innovative/research based problem and **analyze** from engineering view point.	1		
CO-2	Search for related technical material and **understand** the	3		

	content of technical references.			
CO-3	**Define** problem statement and **explore** possible technical solutions.		4,5	
CO-4	**Develop** skill of summarizing technical contents and **organize** the study material in the form of a report.	2		
CO-5	**Present** the work in a systematic way.	2		
CO-6	**Imbibe** professional ethics and moral/societal responsibilities.	6		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	2	2	3

IV Semester

18PDEP400 **Project Phase II** **(0-0-20)22**

Contact Hours: 200

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote team work. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to	**Mapping to POs (1-6)**		
	Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**

CO-1	**Arrive** at an optimal solution towards the problem identified	1		
CO-2	**Design** and **Implement** the algorithm	3,4, 5		
CO-3	**Experiment** on the algorithm developed and **Compare** the results	1,4, 5		
CO-4	**Integrate** the project work carried out in the form of **producing** a technical paper **publication**	2	6	
CO-5	**Organize** the study carried out in a systematic form and prepare the report in a specific format	2	6	
CO-6	**Present** the work in a systematic way	2	6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2