Academic Program: PG

Digital Electronics

Academic Year 2019-20

Syllabus

I & II Semester M. Tech

Department of Electronics and Communication Engineering

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution recognized by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for 1 & 2 semester of PG (Digital Electronics) program in Electronics and Communication Engineering is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering &Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2019-20 till further revision.

Principal Dean (Academic Program) Chairman BOS & HOD

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION:

To develop competent professionals with human values.

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives(PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Design economical, socially relevant and technically sound digital systems based on the principles of Digital Electronics.

PO5: Integrate hardware-software and apply programming practices to realize the solutions in electronics domain.

PO6: Acquire professional and intellectual integrity, ability to conceptualize, solve engineering problems with adherence to professional code of conduct and contribute to sustainable development of society at large.

Scheme of Teaching & Examination for M.Tech Digital Electronics

Scheme for I Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration In hours
18PMAC100	Advanced Mathematics	4-0-0	4	50	100	3		
18PDEC100	Digital Circuits and Logic Design	4-0-0	4	50	100	3		
18PDEE15X	Elective-I	4-0-0	4	50	100	3		
18PDEE15X	Elective –II	4-0-0	4	50	100	3		
18PDEE15X	Elective –III	4-0-0	4	50	100	3		
18PDEL101	Digital Electronics Laboratory-I	0-0-3	2	50			50	3
18PDES103	Seminar**	0-0-3	1	100				
Total		**20-0-6**	**23**	**400**	**500**		**50**	

Elective I to III

18PDEE150	Digital VLSI Design
18PDEE151	Machine Learning
18PDEE152	Digital System Design Using Verilog
18PDEE153	Automotive Electronics
18PDEE154	Nano Electronics
18PDEE155	ASIC Design
18PDEE156	Simulation, Modeling & Analysis
18PDEE157	Advanced Embedded System Design

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination
L: Lecture **T**: Tutorials **P**: Practical

* SEE for theory courses is conducted for 100 marks and reduced to 50 marks.
** Seminar topics should be from emerging areas in Digital Electronics, preferably the contents not studied in their regular courses.

Scheme for II Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration In hours
18PDEC200	Modern DSP	4-0-0	4	50	100	3		
18PDEC201	Coding Theory	4-0-0	4	50	100	3		
18PDEE25X	Elective- IV	4-0-0	4	50	100	3		
18PDEE25X	Elective- V	4-0-0	4	50	100	3		
18PDEE25X	Elective-VI	4-0-0	4	50	100	3		
18PDEPL202	Digital Electronics Laboratory-II	0-0-3	2	50			50	3
18PDEP203	Mini Project	0-0-3	1	100				
Total		**20-0-6**	**23**	**400**	**500**		**50**	

Elective IV to VI

18PDEE250	Advanced Reconfigurable Computing
18PDEE251	System on Chip Design
18PDEE252	Low Power VLSI
18PDEE253	Digital Signal Compression
18PDEE254	Image & Video Processing
18PDEE255	Wavelet Transforms
18PDEE256	Multimedia Communication
18PDEE257	Micro Electro-Mechanical Systems

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination
L: Lecture **T**: Tutorials **P**: Practical

* SEE for theory courses is conducted for 100 marks and reduced to 50 marks.

** Seminar topics should be from emerging areas in Digital Electronics, preferably the contents not studied in their regular courses.

*** Select any three electives from the list.

Total Credits offered for first year: 46

I Semester

18PMAC100	Advanced Mathematics	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course will enable students to, acquaint with principles of linear algebra, calculus of variations, probability theory, random process and apply the knowledge in the applications of electronics and communication engineering sciences.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.	3		
CO-2	Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.	4		
CO-3	To develop the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.		4	6
CO-4	Apply Laplace transform method to solve one-dimensional wave equation.			3
CO-5	Apply Fourier transform to solve Laplace equation, Poisson equation and one-dimensional heat equation.		1	
CO-6	Solve linear and non-linear equations.	1,3		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.5	-	2	2.5	-	1

Pre-requisites: Ordinary differential equation, Matrix operation, Basic probability theory, Differential calculus, Laplace transform of partial derivative and Fourier transform of partial derivative.

Course Contents:

1. **Linear Algebra:** Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations. **10 Hrs.**
2. **Calculus of Variations:** Concept of functional - Eulers equation. functional dependent on first and higher order derivatives, functional dependent variables. Isoperimetric problems- Variation problems with moving boundaries. **10 Hrs.**
3. **Probability Theory:** Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples. **10 Hrs.**
4. **Transform Methods:** Laplace transform methods for one dimensional wave equation – Displacements in a string – Longitudinal vibration of an elastic bar. Fourier transform methods for one dimensional heat conduction problems. Fourier transform methods for Laplace equation and Poisson equation. **10 Hrs.**
5. **Linear and Non Linear Programming:** Simplex Algorithm- Two Phase and Big M techniques – Duality theory- Dual Simplex method. Non Linear Programming –Constrained extremal problems- Lagranges multiplier method- Kuhn- Tucker conditions and solutions. **12 Hrs.**

Reference Books:

1. Richard Bronson, "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2. E. Kreyszig, , "Advanced Engineering Mathematics",10th edition, Wiley, 2015.
3. Elsgolts, L., "Differential Equations and Calculus of Variations", Mir, 1977.

4. Sneddon,I.N., "Elements of Partial differential equations", Dover Publications, 2006.
5. Sankara Rao, K., "Introduction to partial differential equations", Prentice – Hall of India, 1995
6. Taha H A, “Operations research - An introduction", McMilan Publishing co, 1982.
7. T.Veeraranjan: “Probability, Statistics and Random Process”, 3rd Edition, Tata McGraw Hill Co., 2008.
8. Scott L.Miller, Donald G.Childers: “Probability and Random Process with application to Signal Processing” Elsevier Academic Press, 2nd Edition, 2013.

18PDEC100 Digital Circuits and Logic Design (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on threshold logic, fault detection and location in combinational circuits. It also covers the detailed sequential machine minimization procedures, state assignments using partitions, machine decomposition, state identification and fault detection experiments for sequential machines.

Course Outcomes(COs):

Description of the course outcomes: At the end of the course the students will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**List** elementary properties of threshold element and **logic design** of switching circuit by threshold elements	1	4	--
CO-2	**Explain, analyze and design of** different fault detection and fault location experiments for combinational logic circuits and sequential machines.	4	--	2
CO-3	**Analyze** different techniques of failure tolerant design.	4	--	2
CO-4	**Analysis and application** of algorithms for Simplification of completely and incompletely specified sequential machines.			5
CO-5	**Choose** and **adapt** techniques to		1,2	

	decompose the sequential machine into series components, parallel components and to achieve input independency, reduction in the output dependency			
CO-6	**Design** and **Implement** homing experiments, distinguishing experiments and machine identification experiments.		3	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	0.83	0.66	0.33	1.33	0.16	-

Pre-requisites:
Boolean Algebra, Logic Design

Course Contents:

1. **Threshold Logic:** Introductory Concepts, Synthesis of Threshold Networks. **04 Hrs.**
2. **Reliable Design and Fault Diagnosis Hazards:** Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure Tolerant Design, Quadded Logic. **15 Hrs.**
3. **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite - State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. **8 Hrs.**
4. **Structure of Sequential Machines:** Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions, Synthesis of Multiple Machines. **15 Hrs.**
5. **State—Identifications and Fault-Detection Experiments:** Homing Experiments, Distinguishing Experiments, Machine Identification, Fault- Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for **10 Hrs.**

Machines which have no Distinguishing Sequences.

Activity beyond Syllabus:
Seminar/Demonstration, Case studies on various fault detection techniques.

Reference Books:

1. Zvi Kohavi, “Switching and Finite Automata Theory”, 2nd Edition. Tata McGraw Hill Edition
2. Charles Roth Jr., “Digital Circuits and logic Design”, Thomas Asia Pte Ltd., Singapore, 6th Edition, 2004.
3. Parag K Lala, “Fault Tolerant And Fault Testable Hardware Design”, Prentice Hall Inc. 1985
4. E. V. Krishnamurthy,“Introductory Theory of Computer”, Macmillan Press Ltd, 1983.
5. Mishra & Chandrasekaran, “Theory of computer science Automata,Languages and Computation”, 2nd Edition, PHI, 2004.

18PDEL101 Digital Electronics Laboratory-I (0-0-3)2

Contact Hours: 20

Course Learning Objectives (CLOs):
The course focuses on design of digital circuits and verifying the same with Verilog code. Development on FPGA and Cadence tool is also made.

Course Outcomes (COs):

Description of the course outcomes: At the er of the course the students will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Demonstrate** all the logic gate implementation using Verilog code.		1	
CO-2	**Design** different digital circuits and verify the functional simulation.		1	2
CO-3	**Design** digital system verify the functional simulation.		2,3	
CO-4	**Implement** digital circuit and digital system on FPGA board	1,2,3	4,5	6
CO-5	**Develop** layout for digital circuit and digital system.	1,3	4	2,5
CO-6	**Build** and **Implement** application based digital system as a part of Hobby Projects.	1,2,3	4,5	6

Pre-requisites:
Digital Electronics, Verilog HDL

Course Contents:

PART A
FPGA DIGITAL DESIGN

Programming can be done using any complier. Download the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer)/Chip scope pro apart from verification by simulation with any of the frontend tool.

1. Write Verilog code for the design of 8-bit.
   i. Carry Ripple Adder
   ii Carry Look Ahead adder
   iii. Carry Skip Adder

2. Write Verilog Code for 8-bit
   i. Array Multiplication
   ii. Booth Multiplication (Radix-4)

3. Write Verilog code for4/8-bit
   i. Magnitude Comparator
   ii. LFSR

4. Write Verilog Code for 3-bit Arbitary Counter to generate 0,1,2,3,6,5,7 and repeats.

5. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg11101 (with and without overlap) any sequence can be specified.

6. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

PART B
CADENCE DIGITAL DESIGN

Write the Programs for the following experiments using Cadence digital environment. Use NC Verilog Compiler and generating the layout using Encounter

1. Write Verilog code for the design of 8-bit BCD Adder & Subtracter.

2. Write Verilog code for 4/8-bit
   i. Parity Generator
   ii. Universal Shift Register

3. Write Verilog code for 4-bit binary UP/DOWN counter

4. Write Verilog code for the design of
   i. 4- bit RAM
   ii. 5- bit ROM

18PDES103	Seminar	(0-0-3)1

Course Learning Objectives (CLOs):

Seminar is to train students towards studying technical papers, preparing report and presentation of the same.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** technically relevant and innovative topic from refereed technical journals/conferences	1	3	
CO-2	**Understand and analyze** the selected topic.	2	1	
CO-3	**Compare** different techniques relevant to the selected topic.	2		
CO-4	Organize the topic in a systematic manner and **prepare** the report in specific format		2	6
CO-5	**Present** the work in a systematic way.	1, 2		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.75	2.8	2	-	-	1

ELECTIVES I to III

18PDEE150	Digital VLSI Design	(4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

The course focuses on understanding of construction details and electrical characteristics of MOSFETs, designing different digital applications of MOSFETs for the high speed and low power considerations.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Explain the theory, construction and			6

	the characteristics of MOS structures.			
CO-2	Design of an Inverter with different loads.		5,6	
CO-3	Design digital circuits using various design styles.	4,5		6
CO-4	Compare the performance of CMOS and Bi-CMOS logic circuits.		3	
CO-5	Various memory structures and low power design techniques are explored	3,5		
CO-6	Design and validation of digital systems.	3	5,6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	---	---	1.4	3	2	1.3

Pre-requisites: Digital Circuit Design, Basic VLSI Design

Course Contents:

1. **MOS Transistor:** The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **08 Hrs.**
2. **MOS Inverters:** Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter. MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints. **08 Hrs.**
3. **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **06 Hrs.**
4. **Semiconductor Memories**: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Non-volatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM). **08 Hrs.**

5. **Low-Power CMOS Logic Circuits:** Introduction, Overview of Power Consumption, Low-Power Design Through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, Adiabatic Logic Circuits. **08 Hrs.**
6. **Bi-CMOS Logic Circuits:** Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behaviour of BJTs, Basic Bi-CMOS Circuits: Static Behaviour, Switching Delay in Bi-CMOS Logic Circuits, Bi-CMOS Applications. **08 Hrs.**
7. **Chip Input and Output (I/O) Circuits:** Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **06 Hrs.**

Activity beyond syllabus: Design of Digital Circuits using Cadence Software.

Reference Books:

1. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.
2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

18PDEE151 Machine Learning (4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on introduction to the fundamental concepts in machine learning and popular machine learning algorithms. It includes linear modeling, Bayesian approach, classification, clustering and Principal Component Analysis. In the course also discusses various issues related to the application of machine learning algorithms.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** variety of mathematical modeling, inference, and prediction algorithms for machine learning	3	2	
CO-2	**Analyze** the situations of applying	2,3	1	

	variety of mathematical models and algorithms for machine learning			
CO-3	**Compare and justify** mathematical models and algorithms for machine learning	1, 4		2
CO-4	**Apply** algorithms for machine learning and **solve** concerned problems	4, 6		
CO-5	**Justify** the selection of algorithms for machine learning	3	2	
CO-6	**Evaluate** the performance of algorithms for machine learning	3	1	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.3	4	3	3	-	3

Pre-requisites:
Basics of probability and statistics.

Course Contents:

1. **Linear Modeling-A Least Squares Approach:** Linear Modeling, Making Predictions, Vector/Matrix Notation, Non-Linear Response from a Linear Model, Generalization and Over-Fitting, Regularized Least Squares. **06 Hrs.**
2. **Linear Modeling-A Maximum Likelihood Approach:** Errors as Noise, Random Variables and Probability, Popular Discrete Distributions, Continuous Random Variables - Density Functions, Popular Continuous Density Functions, Likelihood, The Bias-Variance Trade-off, Effect of Noise on Parameter Estimates, Variability in Predictions. **08 Hrs.**
3. **The Bayesian Approach to Machine Learning**: A Coin Game, The Exact Posterior, The Three Scenarios, Marginal Likelihoods, Hyper parameters, Graphical Models, A Bayesian Treatment of the Olympic100m Data, Marginal Likelihood for Polynomial Model Order Selection. **08 Hrs.**
4. **Bayesian Inference:** Non-Conjugate Models, Binary Responses, A Point Estimate - The Map Solution, The Laplace Approximation, Sampling Techniques. **07 Hrs.**

5. **Classification:** The General Problem, Probabilistic Classifiers, Non-Probabilistic Classifiers, Assessing Classification Performance, Discriminative and Generative Classifiers. **08 Hrs.**
6. **Clustering:** The General Problem, K-Means Clustering, Mixture Models. **08 Hrs.**
7. **Principal Components Analysis and Latent Variable Models:** The General Problem, Principal Components Analysis, Latent Variable Models, Variational Bayes, A Probabilistic Model for PCA, Missing Values, Non-Real-Valued Data. **07 Hrs.**

Activity beyond Syllabus: Program development for the machine learning Algorithms in MATLAB and Python.

Reference Books:

1. Simon Rogers, Mark Girolami, "A First Course in Machine Learning", CRC Press, 2017.
2. Ethem Alpaydin, "Introduction to Machine Learning", Prentice Hall of India, Third edition, 2014
3. Mohssen Mohammed, Muhammad Badruddin Khan, Eihab Bashier Mohammed Bashier, "Machine Learning, Algorithms and Applications", CRC Press, 2017.
4. Tom Mitchell, "Machine Learning", First Edition, McGraw- Hill, 1997.
5. Michael Paluszek, Stephanie Thomas, "MATLAB Machine Learning", A press, 2017.

18PDEE152 Digital System Design Using Verilog (4-0-0) 4

Contact Hours:52

Course Learning Objectives(CLOs):

Students will learn to analyze and design digital systems comprising both hardware and software components, Design methodology based on using abstraction, to manage complexity along with principles and methods for making design trade off.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** and **Explain** the basic concepts of Digital design by using combinational and sequential circuits using verilog.	2	5	3

CO-2	**Describe** and design the real life applications using verilog		5	
CO-3	**Design** and Diagnosis of processors and controllers which are used in embedded system.	2		4
CO-4	**Design** digital systems by using programmable Logic Devices..			1
CO-5	**Design** and model various types of memories using verilog.		2,3	1
CO-6	**Study and Explain** different fault modeling techniques and optimization.			1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2.5	1.5	1	2	-

Pre-requisites:

1. Knowledge of Digital Circuit Design
2. Knowledge of Verilog

Course Contents:

1. **Introduction and Methodology**: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **10 Hrs.**
2. **Sequential Basics**: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology. **5 Hrs.**
3. **Memories**: Concepts, Memory Types, Error Detection and Correction. **5 Hrs**.
4. **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **7 Hrs.**
5. **Processor Basics**: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **7 Hrs.**
6. **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **7 Hrs.**
7. **Accelerators**: Concepts, case study, Verification of accelerators. **6 Hrs.**

8. **Design Methodology**: Design flow, Design optimization, Design for test. **5 Hrs.**

Activity beyond syllabus:
Assignments, Design of different digital systems using Verilog.

Reference Books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using Verolog", Elsevier, 2010.
2. Charles Roth Jr., " Digital Circuits and Logic Design"

18PDEE153 Automotive Electronics (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):
The course focuses on the concepts of automotive systems, design cycles, automotive sensors and actuators, microprocessors/microcontrollers in automotive domain, communication protocols, infotainment systems, model based development and active and passive safety systems in automobile.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** four stroke engine and engine management system		4	3
CO-2	**Explain** the sensors and sensor monitoring mechanisms aligned to automotive systems, different interfacing techniques and actuator mechanisms		3	1
CO-3	**Describe** the role of electronics in vehicle in fuel control system, EGR and engine management	1	3	4
CO-4	**Explain** various communication systems of automotive system.		5	1
CO-5	**Describe** active, passive safety systems and diagnostics systems of modern automotive systems		5	4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.6	-	1.6	1.3	2	-

Pre-requisites:

Basic Electronic devices and circuits, Basics of transducers, Basics of Mechanical Engineering

Course Contents:

1. **Automotive Fundamentals Overview:** Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System **Air/Fuel Systems** – Fuel Handling, Air Intake System, Air/ Fuel Management. **10 Hrs**.
2. **Sensors and Actuators Sensors:** Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor **12 Hrs.**
   Actuators: Fuel Metering Actuator, Fuel Injector, Ignition Actuator.
3. **Engine Control System**: **Exhaust After-Treatment Systems:** AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems **Electronic Engine Control –** Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control. **10 Hrs**.
4. **Vehicle Communication and Instrumentation Communication:** Serial Data, Communication Systems, Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, GPS **Vehicle Motion Control** – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension **10 Hrs.**
   Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters.
5. **Automotive Safety and Diagnostics Integrated Body:** Climate Control Systems, Electronic HVAC Systems, Safety Systems – SIR, **10 Hrs.**

Interior Safety, Lighting, Entertainment Systems **Automotive Diagnostics** – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems **Future Automotive Electronic Systems** – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System.

Activity beyond syllabus:

Design of Automotive systems using MATLAB and Simulink.

Reference Books:

1. William B. Ribbens, "Understanding Automotive Electronics", 6th Edition, SAMS/Elsevier Publishing.
2. Robert Bosch Gambh, "Automotive Electrics, Automotive Electronics Systems and Components", 5th edition, John Wiley & Sons Ltd., 2007.

18PDEE154	Nano Electronics	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the study of various nanostructures, their properties and applications. The course also focuses on understanding the physical, chemical and fabrication aspects of nanostructures at nanoscale, relevant to the field of electronics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping of POs(1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Understand and appreciate the significance of Nano-electronics, as an emerging area in the field of electronics.	1	3	-
CO-2	Identify various nanostructures, discuss their properties and applications	1	-	3
CO-3	Analyze and discuss the physical effects occurring in various Nano devices.	-	-	3

CO-4	Classify different microscopic techniques required to study novel properties of nanostructures occurring at Nano scale.	-	1	-
CO-5	Compare and differentiate various quantum structures, self assembly techniques.	-	2	-
CO-6	Discuss the applications of nanostructures, in relevance to the field of electronics.	-	1,3	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2	2	1.5	-	-	1

Pre-requisites:
Physics, Electronics, Engineering Mathematics, Material Science

Course Contents:

1. **Introduction:** Overview of nanoscience and engineering, development milestones in micro fabrication and electronic industry, Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes for the growth of Nano materials, ordering of Nano systems. **6 Hrs.**
2. **Characterization**: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, Diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and depth profiling: electron, mass, Ion beam, Reflectrometry, techniques for property measurement: mechanical, electron, magnetic, thermal properties. **8 Hrs.**
3. **Inorganic Semiconductor Nanostructures**: Overview of semiconductor physics, Quantum confinement in semiconductor nanostructures: Quantum wells, Quantum wires, Quantum dots, Super-lattices, band offsets, electronic density of states. **8 Hrs.**
4. **Fabrication techniques**: Requirements of ideal semiconductor, **8 Hrs.**

epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.

5. **Physical processes:** Modulation doping, Quantum Hall effect, Resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined Stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical, electrical and structural. **8 Hrs.**
6. **Methods of measuring properties-structures:** Atomic properties, crystallography, microscopy, spectroscopy. Properties of nanoparticles: metal nano clusters, semiconducting nanoparticles, rare gas and molecular clusters, methods of synthesis (RF, chemical, thermolysis, pulsed laser methods). Carbon nanostructures and its applications. Self assembling nanostructured molecular materials and devices: building blocks, principles of self assembly, methods to prepare and pattern nano particles. Nanomagnetic materials and devices: magnetism, materials, magnetoresistance, nanomagnetism in technology, challenges faced in nanomagnetism. **8 Hrs.**
7. **Applications**: Injection lasers, quantum cascade lasers, single photon sources, optical memories, Coulomb blockade devices, photonic structures, NEMS, MEMS. **6 Hrs.**

Reference Books:

1. Ed. Robert Kelsall, Lan Hamley, Mark Geoghegan, “Nano scale science and technology”, John Wiley and sons, 2007.
2. Charles P Poole, Jr. Frank J. Owens, “Introduction to Nanotechnology”, John Wiley, copyright 2006, Reprint 2011.
3. Ed. William, A Goddard III, Donald W. Brenner, Sergey Edward Lyshevski, Gerald J. Lafrate, “Hand Book of Nano science Engineering and Technology”,
   CRC press, 2003.

18PDEE155	ASIC Design	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

ASIC Design course focuses on study of Data logic cells, Library cell design and Low level design. The course also emphasis on algorithms on Floor planning, Placement and routing of programmable logic arrays.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping of POs(1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** the principles and characteristics of Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC.			6
CO-2	**Distinguish** and **compare** performances various ASIC Systems including cells		4,5	3
CO-3	**Design** and **development** of ASIC Library cells, Low level Design	4,5		
CO-4	**Implement** system design using Low level Design Language	5	3	
CO-5	ASIC Floor planning **construction** and **realization**		3	
CO-6	**Development** of routing algorithms		3,4	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	-	-	2.2	2.3	2.6	1

Pre-requisites:

Basics of digital Logic, VLSI Design and HDL

Course Contents:

1. **Introduction**: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channelled **9 Hrs.**

gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, SIC cell libraries.

2. **Data Logic Cells:** Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers **13Hrs.**
3. **Low-Level Design Entry:** Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation. Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell **13Hrs.**
4. **A Brief Introduction to Low Level Design Language:** an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation. **10Hrs.**
5. **ASIC Construction Floor Planning and Placement and Routing:** Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement,Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC. **7Hrs.**

Reference Books:

1. M.J.S .Smith, "Application - Specific Integrated Circuits", Pearson Education, 2003.

2. Jose E.France, YannisTsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", Prentice Hall, 1994.

18PDEE156 Simulation Modeling and Analysis (4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

The objective of this course is to introduce simulation modeling and analysis and focus on the methodology needed for successful simulation. There will be no simulation language used in this course, although a few software demonstrations will be given. At the end of the course, you will understand how simulation works, how to model a system using simulation, how to evaluate the output of any simulation software, and how to use it to compare and optimize system performance.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping of POs(1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** and **identify** different simulation models and their applicability.	1	3	
CO-2	**Build** valid and credible simulation models.	4	2,3	
CO-3	**Asses and build** a model for input generation maintaining sample independence and arrival process.	1, 2		5
CO-4	**Understand** and **utilize** randomization process while building simulation model		1	5
CO-5	**Interpret** the data using statistical methods.	2		
CO-6	**Compare and Comprehend** system configurations.		6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.67	2.67	2	3	2	2

Pre-requisites:

Knowledge of simulation tools as well as HLL is appreciated.

Course Contents:

1. **Basic simulation modeling:** Nature of simulation, System models, discrete event simulation, Steps in sound simulation, modeling complex system, List Processing in simulation, Simple simulation language: simlib. **6 Hrs.**
2. **Building valid, credible and detailed simulation models**: Introduction and definitions, Guidelines for determining the level of model detail, Verification of simulation computer programs, Techniques for increasing model validity and credibility **7 Hrs.**
3. **Selecting input probability distributions:** Useful probability distributions, Assessing sample independence, Activity-I, II and III, Selecting the distribution in the absence of data, Assessing the homogeneity of difference data sets. **10 Hrs.**
4. **Random number generators:** Linear congruential, Other kinds, Testing number generators, Random variate generation: **7 Hrs.**

Approaches, Continuous random variates, Discrete random variates, Correlated random variates.

5. **Output data analysis:** Transient and steady state behavior of stochastic Process, Types of simulations with regard to output analysis, Statistical Analysis of terminating simulations, statistical analysis of for steady state parameters, Statistical analysis for steady state cycle parameters, Multiple measures of Performance. **8 Hrs.**
6. **Comparing and Optimizing Systems:** Comparing alternative system configurations, Confidence Intervals for the difference between the expected response of two systems, Confidence intervals for comparing more than two systems, Ranking and selection, Experimental Design and Optimisation,2^k factorial designs,2^{k-p} Fractional Factorial Designs, Response surfaces and meta models, Simulation based Optimization. **9 Hrs.**
7. **Variance-reduction Techniques: Common** random numbers, Antithetic Variates, Control Variates, Indirect estimation, Conditioning. **5 Hrs.**

Reference Books:

1. Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.
2. Jerry Banks, "Discrete event system Simulation", Pearson, 2009.
3. Seila Ceric and Tadikamalla, "Applied simulation modeling", Cengage, 2009.
4. George. S. Fishman, "Discrete event simulation", Springer, 2001.
5. Frank L. Severance, "System modeling and simulation", Wiley, 2009.

18PDEE157 Advanced Embedded System Design (4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

The course focuses on real time task scheduling, modifications required in multiprocessor environment, handling of resource sharing and database requirements. Knowledge of General Embedded system and Operating System is required as prerequisite.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping of POs(1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Identify the principles and characteristics of various	3		1

	applications of Basic and advanced ES.			
CO-2	Distinguish and compare performances various Embedded systems.		3,4	2
CO-3	Design and development of Embedded Systems	1		
CO-4	Architecture and programming concepts of 32-bit Micro controller family.		4	5
CO-5	Embedded System Design based on RTOS.		5	
CO-6	Development of IDE for Design of Advanced ES.	6		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	2.5	2	1.5	3

Course Contents:

1. **Typical Embedded System: Core** of the Embedded System, Memory, Sensors and Actuators, Communication Interface, **8 Hrs.**
2. **Embedded Hardware Design and Development**: EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement, PCB track routing. **14 Hrs.**

   Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages.
3. **ARM -32 bit Microcontroller family :** Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture. **12 Hrs**.

4. **Real-Time Operating System (RTOS) based Embedded System Design** : Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device **10 Hrs.**
5. **The Embedded System Development Environment**: The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan. **8Hrs.**

Activity beyond syllabus:

Case study and Implementation of RTES.

Reference Books:

1. Shibu K. V., “Introduction to Embedded Systems”, Tata McGraw Hill Education Pvt. Ltd.,, 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Newnes, (Elsevier), 2008.
3. James K Peckol, “Embedded Systems – A contemporary Design Tool”, John Weily, 2008.

II Semester

18PDEC200 Modern DSP (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on some of the modern techniques in signal processing such as multi rate signal processing, signal transforms and nonlinear filters and adaptive filters.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Analyze and outline** the principles of multi rate signal processing techniques	2, 3		
CO-2	**Apply** mathematical concepts of signal transformations.	3	1, 6	4
CO-3	**Determine** system response for different filters given signal / situation.	6		
CO-4	**Analyze** the principles of nonlinear digital filters.	2, 3		1
CO-5	**Evaluate** the performance of nonlinear digital filters.	6		
CO-6	**Analyze** adaptive filtering techniques and their applications.	2,3		1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	1.3	3	3	1	-	2.6

Pre-requisites: Digital Signal Processing

Course Contents:

1. **Fundamentals of Multirate Systems**: Introduction, Basic Multirate Operations, Interconnection of Building Blocks, The Polyphase Representation, Multistage Implementations, Applications of Multirate Systems. **08 Hrs.**
2. **Maximally Decimated Filter Banks**: Introduction, Errors created in the QMF Bank, A Simple Alias Free QMF System, M-Channel Filter **10 Hrs.**

Banks, Polyphase Representation, Perfect Reconstruction Systems, Alias Free Filter Banks, Transmultiplexers, Applications.

3. **Two Dimensional Transforms:** Introduction, Unitary Transforms, 2-D DFT, Cosine Transform, Sine Transform, Hadamard Transform, Haar Transform, KL Transform. **08 Hrs.**
4. **Nonlinear Digital Filtering:** Signal Modeling, Trimmed Mean Filters, L-Filters, C-Filters, Weighed Median Filters, Ranked-Order and Weighed Order Statistic Filters, Multistage Median Filters, Median Hybrid Filters, Edge-Enhancing Selective Filters, Rank Selection Filters, M-Filters, R-Filters, Nonlinear Mean Filters **10 Hrs.**
5. **Introduction to Adaptive filter:** Three kinds of estimation, Adaptive filter, Approaches to the development of Linear Adaptive filter, Applications of Adaptive Filters. **06 Hrs.**
6. **Linear Adaptive Filter:** the filtering problem, linear optimum filters, adaptive filters, linear filer structures, approaches to linear adaptive filters, adaptive beam forming, 4 classes of applications, LMS Adaptive Filters, Overview of the structure & operation of LMS algorithm, LMS algorithm, Applications of LMS algorithm. RLS Adaptive Filters, preliminaries, exponentially weighted recursive least squares algorithm, selection of the regularization parameter, update recursion for the sum of weighted error squares, example single weight adaptive noise canceller. **10Hrs.**

Activity beyond Syllabus: Implementation of Signal Processing concepts using software platform for practical data input.

Reference Books:

1. P. P. Vaidyanathan, “Multirate systems and filter banks”, Prentice Hall, 1993.
2. Jaakko Astola, Pauli Kuosmanen, “Fundamentals of Nonlinear Digital filtering”, CRC Press.
3. Simon Haykin, “Adaptive Filter Theory”, 4th Edition, Pearson Education.
4. S. V. Narasimhan, S Roopa& S. Veena, “Optimum and Adaptive Signal Processing”, IK International Publishing House, 2016.

18PDEC201	Coding Theory	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives(CLOs):

Coding Theory is a core course at II semester level with 4 credits (LTP: 4-0-0-0) to be covered in 52 Hrs. Knowledge of information theory and coding is required as prerequisite. The course focuses on various error detection and error correction coding techniques.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Apply** and **calculate** Galois field arithmetic for error control coding techniques in digital communication and data storage systems		1	
CO-2	**List** and **state** structural, distance properties of error control codes.		1	3
CO-3	**Explain** and **analyze** different error control codes like, Linear block codes, cyclic codes, BCH codes, MLD codes, convolution codes, Concatenated, Turbo, LDPC codes and burst error correcting codes		2	
CO-4	**Design** and **Implement** different error control codes.	4		5,6
CO-5	**Choose** and **adapt** error control coding techniques for different applications.		1	
CO-6	**Analyze** decoder performance.	3		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2	2	2	3	1	1

Pre-requisites: Knowledge of Information Theory & coding, Digital Communication.

Course Contents:

1. Introduction to Algebra: Groups, Fields, Binary Field Arithmetic, Construction of Galois Field GF (2m) and its basic properties, Computation using Galois Field GF (2m) Arithmetic, Vector spaces and Matrices. **10 Hrs.**
2. Linear Block Codes: Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Hamming Codes, Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes. **06 Hrs.**
3. Cyclic Codes: Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes – Encoding using Feedback shift register circuits, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, The (23, 12) Golay code, Shortened cyclic codes. **10 Hrs.**
4. BCH Codes and Majority Logic Decodable Codes : Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Reed – Solomon Codes, One – Step Majority logic decoding, one – step Majority logic decodable Codes, Two – step Majority logic decoding. **12 Hrs.**
5. Convolution Codes: Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Stack and Fano sequential decoding Algorithms. **8 Hrs.**
6. Concatenated Codes & Turbo Codes: Single level Concatenated codes, Multilevel Concatenated codes, s, Introduction to Turbo coding and their distance properties, Design of Turbo codes. **6 Hrs.**

Activity beyond Syllabus: Assignments on the design of various coding techniques.

Reference Books:

1. Shu Lin & Daniel J. Costello, Jr. “Error Control Coding”, Pearson / Prentice Hall, Second Edition, 2004.
2. Blahut, R.E., “Theory and Practice of Error Control Codes”, Addison Wesley, 1984.
3. Satyanarayana P.S., “Concepts of Information Theory & coding”, Dynaram Publications, Bangalore, 2005.
4. Ranjan Bose, “Information Theory, Coding and Cryptography”, Tata McGraw-Hill Publication, 2002, ISBN: 0-07-048297-7

18PDEPL202	Digital Electronics Laboratory-II	(0-0-3)2

Contact Hours:36

Course Learning Objectives(CLOs):

The course focuses on the study of various Digital circuits using LabVIEW and different applications for embedded systems using NXP LPC1768.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Design and Realize** Combinational Circuits			2,3
CO-2	**Build** various flip flops using basic gates to **Realize** them as memory elements.		2,5,6	
CO-3	**Demonstrate** programming skills using Assembly Level Language and High Level Language such as C	2,5,6		
CO-4	**Extrapolate** Interrupt Service Routine (ISR) for various sources of interrupts.		5,6	
CO-5	**Demonstrate** the usage and importance of Inter Process Communication(IPC)		5,6	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	1	1	-	1.8	1.8

Pre-requisites:

1. Digital Circuit design
2. Programming language

List of Experiments

i. Design of 4 bit Adders and Subtractors
ii. Design of Encoder, Decoder, Multiplexer and Demultiplexer
iii. Design of code converters and comparators
iv. Design of Flip-flops
v. Design of registers using flip-flops
vi. Write an Assembly language program to calculate 10+9+8+…+1

vii. Write an Assembly language program to link Multiple object files and link them together.
viii. Write an Assembly language program to store data in RAM
ix. Write C program to output “Hello World” message using UART
x. Write C program to design a stopwatch using interrupts

Reference Books:

1. Donald D Givone, “Digital Principles and Design”. Tata McGraw Hill Edn, 2003.
2. Charles H. Roth, “ Fundamentals of logic design”, Thomson Learning, 2004.
3. Joseph Yiu, “The Definative Guide to ARM Cortex-M3”, Newenes Publication

18PDEP203 Mini Project (0-0-3)1

Contact Hours: 36

Course Learning Objectives(CLOs):

The course concentrates on selection of mini project work based on student’s interest and their knowledge in the technical domain.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** a socially and technically relevant problem	1, 6		
CO-2	**Understand** the content of technical references and **summarize** the same.	1, 2		3
CO-3	**Analyze** the content matter of the technical papers and **formulate** better solution.	2	3, 6	
CO-4	**Train** oneself in recent technological trends	1, 4, 5	3	
CO-5	**Choose** techniques to carry out the project work	6	4, 5	
CO-6	**Organize** the study carried out in a systematic form	1, 2		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	1.6	2.5	2.5	2.6

ELECTIVES IV to VI

18PDEE250 Advanced Reconfigurable Computing (4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

Reconfigurable Computing is an elective theory course at postgraduate II semester level. Knowledge of design based on FPGA and microcontroller architecture are required as prerequisites. The course focuses on key criteria: power, area, speed, optimization techniques employed, various system architectures considered in the design of digital circuits.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** the basics of computing required for processor speed	4	3	1,2
CO-2	**Explain** the technique of reconfiguration required for RTL synthesis	4	2,3	1
CO-3	**Simulate** and **synthesize** the reconfigurable computing architectures.	3	5,2	1
CO-4	**Analyze** and use the reconfigurable architectures for the design of a digital system.	3	1	5,2
CO-5	**Design** of digital systems for a variety of applications on signal processingan d system on chip configurations.	4,2		1
CO-6	**Analyze** the applications of reconfigurable computing applications.	4	1,2	3

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	1.33	1.83	2.6	3.0	1.5	-

Pre-requisites:
Algorithms, Verilog & VHDL Basics

Course Contents:

1. **Introduction:** History, Reconfigurable Vs Processor based system, RC Architecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. **Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing **10 Hrs**
2. **Languages and Compilation:** Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. **10 Hrs**
3. **Implementation:** Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices:** Modelling,Temporal Partitioning Algorithms. **10 Hrs**
4. **Partial Reconfiguration Design:** Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design. **10 Hrs**
5. **Signal Processing Applications:** Reconfigurable computing for DSP, DSP application building blocks, Examples: Beam-forming, Software Radio, Image and video processing, Local Neighborhood functions, Convolution. **12 Hrs**
   System on a Programmable Chip: Introduction to So PC, Adaptive Multiprocessing on Chip.

Activity beyond Syllabus:

1. Simple examples may be given on the various concepts/algorithms for better understanding of the subject.
2. Mini project on Image processing using Reconfigurable Hardware

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Reference books:

1. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
2. C. Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2007.
3. D. Pellerin and S. Thibault, “Practical FPGA Programming in C”, Prentice-Hall, 2005.
4. W. Wolf, “FPGA Based System Design”, Prentice-Hall, 2004

5. R. Cofer and B. Harding, “Rapid System Prototyping with FPGAs: Accelerating the Design Process”, Newnes, 2005.

18PDEE251 System on Chip Design (4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

Today, VLSI chips are entire “system-on-chip” designs, which include processors, memories, peripheral controllers, and connectivity sub-systems. The course aims to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** the basics of CMOS and SOC.	1		
CO-2	**Analysis** of circuits with equations for performance Maximization.	2,3	1	6
CO-3	**Modeling** of Design flow with types of SOC with timing issues	4	1	6
CO-4	**Design** of cache memory, Flash memory with MESI protocol.	2,3,5	4	1
CO-5	**Analyze** the Bus architectures for NOC communication.	2,3	1	
CO-6	**Evaluate and Design** of MpSOC’s with case study of application.	2,3	1	4

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.0	3.0	3.0	2.0	3.0	1.0

Pre-requisites:

Basics of Analog Electronics, Engineering Mathematics, CMOS Basics.

Course Contents:

1. **Motivation for SoC Design** - Review of Moore‟s law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to **10 Hrs.**
2. **System On Chip Design Process:** A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc. **10 Hrs.**
3. **Embedded Memories –**cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache **10 Hrs.**
4. **Interconnect architectures for SoC. -** Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole **08 Hrs.**
5. **MPSoCs:** What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design **08 Hrs.**
6. **Case Study:** A Low Power Open Multimedia Application Platform for 3G Wireless**.** **06 Hrs.**

Activity beyond Syllabus:

1. Seminar on related SOC Architectures.
2. Theme Based Projects

Reference Books:

1. Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
2. Rao R. Tummala, Madhavan Swaminathan, "Introduction to system on package sop- Miniaturization of the Entire System", McGraw-Hill, 2008.
3. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition.
4. Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System on Chip designs", Kluwer Accademic Publishers, 2nd edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", Tata Mcgraw-Hill, 3rd Edition.

18PDEE252	Low Power VLSI	(4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

course will enable students to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays a major role. Describe the various power reduction and the power estimation methods. Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system. Apply State-of-the art approaches to power estimation and reduction. Practice the low power techniques using current generation design style and process technology

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Identify the sources of power dissipation in CMOS circuits.		5,6	
CO-2	Perform power analysis using simulation based approaches and probabilistic analysis.	3,6		5
CO-3	Use optimization and trade-off techniques that involve power dissipation of digital circuits.		3,5	6
CO-4	Make the power design a reality by making power dimension an integral part of the design process	6	3	
CO-5	Use practical low power design techniques and their analysis at various levels of design abstraction and analyze how these are being captured in the latest design automation environments.		3,5	
CO-6	Apply the low power techniques to build efficient system.	4,5		6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	-	2.5	3	2.7	2.5

Pre-requisites:

Digital VLSI Design

Course Contents:

1. **Introduction:** Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS circuit, CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **6 Hrs**
2. **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **6 Hrs**
3. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **5 Hrs**
4. **Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. **5 Hrs**
5. **Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **5 Hrs**
6. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network . **5 Hrs**
7. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation. **5 Hrs**
8. **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division. **5 Hrs**
9. **Low power memory design:** Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM. **5 Hrs**
10. **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.**Advanced Techniques:** Adiabatic computation, pass transistor logic synthesis, Asynchronous circuits. **5 Hrs**

Activity beyond syllabus: Power simulation at gate level, logic level and architectural level assignments using Spice tool.

Reference Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.

2. Jan M.Rabaey, Massoud Pedram, "Low Power Design Methodologies" Kluwer Academic, 2010.

3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000

4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.

5. A Bellamour and M I Elmasri, " Low power VLSI CMOS circuit design", Kluwer Academic,1995.

18PDEE253	**Digital Signal Compression**	**(4-0-0) 4**

Contact Hours:52

Course Learning Objectives(CLOs):

The subject focuses on principles of coding and compression techniques and their performance measures.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** various compression techniques and **design** signal modeling**.**	2	3	
CO-2	**Understand** the principles of various quantization methods.	1, 3		
CO-3	**Explain** various differential encoding methods.		2, 3	
CO-4	**Analyze** various transform coding methods.		1, 3	
CO-5	**Understand** analysis / synthesis schemes for speech compression.	6		
CO-6	**Explain** various speech, image and video compression standards.	6	4	

CO-7	**Describe** various lossless coding methods.	6	4	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.5	2.5	2.25	2	-	3

Pre-requisites:

Knowledge of Information theory and coding.

Course Contents:

1. **Introduction:** Compression techniques, Modeling & coding, Distortion criteria **03Hrs**
2. **Quantization:** Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Trellis coded quantization. **10Hrs**
3. **Differential Encoding:** Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation. **6 Hrs**
4. **Transform Coding:** Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression. **8 Hrs**
5. **Analysis/Synthesis Schemes:** Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression. **6 Hrs**
6. **Video Compression:** Motion compensation, Video signal representation, Algorithms for video conferencing & videophones – H.261, H. 263, Asymmetric applications – MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video. **7 Hrs**
7. **Lossless Coding:** Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Dictionary techniques – LZ77, LZ78, Applications of LZ78 – JBIG, JBIG2, Predictive coding – Prediction with partial match, Burrows Wheeler Transform, Applications – CALIC, JPEG-LS. **12Hrs**

Activity beyond syllabus:

Modeling of multimedia compression techniques.

Reference books:

1. K. Sayood, “Introduction to Data Compression," Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.
2. N. Jayant and P. Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video,” Prentice Hall, USA, 1984.
3. D. Salomon, “Data Compression: The Complete Reference”, Springer, 2000.
4. Z. Li and M.S. Drew, “Fundamentals of Multimedia,” Pearson Education (Asia) Pvt. Ltd., 2004.

18PDEE254	Image and Video Processing	(4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

Image and Video Processing is an elective course offered at II semester PG level. To learn this subject student should have prior knowledge of Digital signal processing and engineering mathematics. The course focuses on image sampling, quantization, various image enhancement techniques in spatial and frequency domain, color image processing, image compression and fundamental concepts in video processing.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to PO (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** image perception and color vision model.			1
CO-2	**Compute** image transforms with different transformation techniques	3	2	1
CO-3	**Apply** suitable enhancement and restoration techniques for image processing.			1,5
CO-4	**Differentiate** between various filtering techniques in image processing.		2,3	1,5
CO-5	**Choose** appropriate feature extraction techniques for analyzing the given image.		2	1,5
CO-6	**Select** appropriate compression		2	1

	techniques for various image processing applications.			
CO-7	**Describe** various video processing techniques.			1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	1.75	2.0	-	1.0	-

Pre-requisites: Digital signal processing**,** Stochastic and random process Engineering Mathematics.

Course Contents:

1. **Image Perception:** Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. **06 Hrs**
2. **Image Sampling and Quantization:** Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. **04 Hrs**
3. **Image Transforms:** Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform. **06 Hrs**
4. **Image Enhancement:** Point operations, Histogram modeling, Spatial operations, Transform operations, Multi-spectral image enhancement, False color and pseudo-color, Color Image enhancement. **08 Hrs**
5. **Image Filtering & Restoration:** Image observation models, Inverse & Wiener filtering, Fourier domain filters, Smoothing splines and interpolation, Least squares filters, Generalized inverse, SVD and iterative methods, Maximum entropy restoration, Bayesian methods. **08 Hrs**
6. **Image Analysis & Computer Vision:** Spatial feature extraction, Transform features, Edge detection, Boundary extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification techniques. **08 Hrs**

7. **Image Data Compression:** Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, Coding of two tone images, Image compression standards. **06 Hrs.**
8. **Video Processing:** Fundamental concepts in video – Types of video signals, Analog video, Digital video, Color models in video, Video compression techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. **06 Hrs.**

Activity beyond Syllabus:

Seminar, Simulation based Project.

Reference books:

1. Anil K. Jain, “Fundamentals of Digital Image Processing, " Pearson Education (Asia) Pvt. Ltd., Prentice Hall of India, 2004.
2. Z. Li and M.S. Drew, “Fundamentals of Multimedia”, Pearson Education (Asia) Pvt. Ltd., 2004.
3. R. C. Gonzalez and R. E. Woods, “Digital Image Processing”, 2nd edition, Pearson Education (Asia) Pvt. Ltd, Prentice Hall of India, 2004.
4. M. Tekalp, “Digital Video Processing”, Prentice Hall, USA, 1995.

18PDEE255	Wavelet Transforms	(4-0-0) 4

Contact Hours :52

Course Learning Objectives (CLOs):

Wavelet Transforms is an elective theory course at postgraduate II semester level. Knowledge of Signals and Systems is required as prerequisite. The course focuses on Multi Resolution Analysis and Wavelet concepts, wavelet transform in both continuous and discrete domain, applications of Wavelet transform.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** where Fourier analysis fails and where wavelets are preferable.		1	
CO-2	**Gain knowledge** about MRA and representation using wavelet bases.	1, 3		
CO-3	**Acquire knowledge** about various continuous wavelet transforms and design wavelet transform.	3	2	

CO-4	**Acquire knowledge** about various discrete wavelet transforms and design wavelet transform.	3		
CO-5	**Identify** which wavelets and what wavelet properties are appropriate for a given problem/application.	3	1	
CO-6	**Apply wavelet transform** for various signal & image processing applications.	6		

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.3	2	3	-	-	3

Pre-requisites:

1. Signals and Systems
2. Digital Signal Processing

Course Contents:

1. **Fundamentals:** Vector Spaces, Properties, Dot Product, Basis, Dimension, Orthogonality and Orthonormality, Relationship Between Vectors and Signals, Signal Spaces, Concept of Convergence, Hilbert Spaces for Energy Signals, Fourier Theory: Fourier series expansion, Fourier transforms, Short time Fourier transforms, Time frequency analysis. **06 Hrs.**
2. **Multi resolution analysis**: Definition of Multi Resolution Analysis (MRA), Haar Basis, Construction of General Orthonormal MRA, Wavelet Basis for MRA, Continuous Time MRA Interpretation for the DTWT, Discrete Time MRA, Basis Functions for the DTWT, PRQMF Filter Banks. **10 Hrs.**
3. **Continuous wavelet transforms**: Wavelet Transform, Definition and Properties, Concept of Scale and its Relation with Frequency, Continuous Wavelet Transform (CWT), Scaling Function and Wavelet Functions, (Daubechies Coiflet, Mexican Hat, Sinc, Gaussian, Bi Orthogonal), Tiling of Time – Scale Plane for CWT. **12 Hrs**.
4. **Discrete wavelet transform**: Filter Bank and Sub Band Coding Principles, Wavelet Filters, Inverse DWT Computation by Filter Banks, Basic Properties of Filter Coefficients, Choice of Wavelet Function Coefficients, Derivations of Daubechies Wavelets, Mallat's **12 Hrs.**

Algorithm for DWT, Multi Band Wavelet Transforms, Lifting Scheme, Wavelet Transform Using Polyphase Matrix Factorization, Geometrical Foundations of Lifting Scheme, Lifting Scheme in Z – Domain.

5. **Applications**: Wavelet methods for signal processing, Image Compression Techniques: EZW, SPHIT Coding, Image Denoising Techniques: Noise Estimation, Shrinkage Rules, Shrinkage Functions, Edge Detection and Object Isolation, Image Fusion, and Object Detection. **12 Hrs.**

Reference Books:

1. Rao R.M. and A.S. Bopardikar, “Wavelet Transforms Introduction to theory and Applications”, Pearson Education, Asia, 2000.
2. L. Prasad & S.S.Iyengar, “Wavelet Analysis with Applications to Image Processing”, CRC Press, 1997.
3. Soman K.P. and Ramachandran K.I., “Insight into Wavelets From Theory to practice”, Prentice Hall, 2004.
4. J. C. Goswami and A. K. Chan, “Fundamentals of wavelets: Theory, Algorithms and Applications", Wiley Interscience Publication, John Wiley & Sons Inc., 1999.
5. Stephen G. Mallat, “A wavelet tour of signal processing" 2nd Edition Academic Press, 2000
6. M. Vetterli, J. Kovacevic, “Wavelets and subband coding" Prentice Hall Inc, 1995.

18PDEE256	Multimedia Communication	(4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course deals with the understanding quantitative principles guiding the Multimedia Communication. It focuses on data/information representation. Addresses representation standards and compression algorithms. Understanding the requirements Multimedia operating systems. Understand and analyze synchronization concept across network, as well as choice of appropriate network protocols and standards to meet QOS.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Understand** information	1,2,3	4	

	representation, **analyze and choose** information representation based on QOS requirements			
CO-2	**Identify and address** data formats, compression standards and methodologies	1, 2	3	4
CO-3	**Comprehend** MPEG4 video standard		1,2,3	
CO-4	**Visualize** notion of synchronization in Multimedia Communication**.**	1,3		
CO-5	**Understand and inspect** multimedia communication across different networks and protocols	2	4	
CO-6	**Understand and analyze** requirements of multimedia operating systems.		3,4	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2	2.5	-	1	-	-

Pre-requisites:
Knowledge of Processor/Controllers, Languages-Compilers is appreciated.

Course Contents:

1. **Multimedia Communications**: multimedia information representation, multimedia networks, multimedia applications, network QoS and application QoS. **4 Hrs.**
2. **Information Representation:** text, images, audio and video, Text and image compression, compression principles, text compression, image compression. Audio and video compression, audio compression, video compression, video compression principles, video compression standards: H.261, H.263, P1.323, MPEG 1, MPEG 2, Other coding formats for text, speech, image and video. **12 Hrs.**
3. **Detailed Study of MPEG 4**: coding of audiovisual objects, MPEG 4 systems, MPEG 4 audio and video, profiles and levels. MPEG 7 standardization process of multimedia content description, MPEG 21 multimedia framework, Significant features of JPEG 2000, MPEG 4transport across the Internet. **4 Hrs.**

4. **Synchronization:** notion of synchronization, presentation requirements, reference model for synchronization, Introduction to SMIL, Multimedia operating systems, Resource management, process management techniques. **8 Hrs.**
5. **Multimedia Communication Across Networks:** Layered video coding, error resilient video coding techniques, multimedia transport across IP networks and relevant protocols such as RSVP, RTP, RTCP, DVMRP, multimedia in mobile networks, multimedia in broadcast networks. **6 Hrs.**

Reference Books:

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004.
3. Raif steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and applications", Pearson education, 2002
4. Tay Vaughan, "Multimedia: Making it work", 6th edition, Tata McGraw Hill, 2004.
5. John Billamil, Louis Molina, "Multimedia: An Introduction", PHI, 2002
6. Pallapa Venkataram, "Multimedia Information Systems", Pearson education, 2005.

18PDEE257 Micro Electro-Mechanical Systems (4-0-0)4

Contact Hours: 52

Course Learning Objectives(CLOs):

MEMS (Micro-Electro Mechanical Systems)is an elective course at postgraduate II semester level. The course focuses on the study of various electromechanical sensors, actuators and their transduction principles at micro and nanoscale. The course is interdisciplinary in nature and covers the advanced domains of electronics, material science and mechanics at research level.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	Understand and appreciate the significance of MEMS, as an emerging area in the field of electronics.	1	-	2

CO-2	Identify various micro sensors and actuators being used for electromechanical applications.	2	-	4
CO-3	Discuss the processes involved in the fabrication of different micro sensors and micro actuators.	-	2	5
CO-4	Model and Design simple micro sensors and actuators using CAD softwares and perform simulations.	5	2,3	-
CO-5	Classify various micro system packaging technologies related to MEMS	2	3	-
CO-6	Appreciate the technological changes involved in the transformation from MEMS to next generation NEMS.	-	2	

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	2	2	1	1	-

Pre-requisites:

1. Physics
2. Electronics
3. Engineering Mathematics
4. Material Science
5. Basic Mechanical principles

Course Contents:

1. **Overview of MEMS & Microsystems**: MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications. **08 Hrs.**
2. **Scaling Laws in Miniaturization:** Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer. **08 Hrs.**

3. **Transduction Principles in MEMS & Microsystems:** **08 Hrs.** Introduction, Micro sensors — thermal, radiation, mechanical, magnetic and bio — sensors, Micro actuation, MEMS with micro actuators.
4. **Microsystems Fabrication Process:** Introduction, **12 Hrs.** Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro-machining, bulk micromachining, LIGA process, LASER micro machining, MUMPS, FAB-less fabrication.
5. **Micro System Design and Modeling:** Introduction, Design **08 Hrs.** considerations: Process design, Mechanical design, Modeling using CAD tools: ANSYS / Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, Design considerations of Optical MEMS (MOEMS), Design and Modeling: case studies - i) Cantilever beam ii) Micro switches
6. **Micro system packaging:** Over view of mechanical packaging of **08 Hrs.** micro electronics micro system packaging, Interfaces in micro system packaging, Packaging technologies

Reference Books:

1. Tai Ran Hsu, “MEMS and Micro Systems : Design and Manufacture”, Tata McGraw Hill, 2002
2. Boca Raton, “MEMS and NEMS: Systems, Devices and Structures” , CRC Press, 2002
3. J. W. Gardner and V. K. Vardan, “Micro Sensors MEMS and SMART Devices”, John Wiley, 2002 N. Maluf, “Introduction to Micro Mechanical Systems Engineering, Artech House”, Norwood, MA, 2000.