Academic Program: UG

Academic Year 2020-21

Syllabus

III & IV Semester B.E.

Electronics & Communication Engineering

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for III & IV semester of UG program in Electronics and Communication Engineering is recommended by Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2020-21 till further revision.

Chairman BOS & HOD

Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College – Vision and Mission

VISION:

To develop competent professionals with human values

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department- Vision and Mission

Vision

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

Mission

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, effective teaching learning process and the best of laboratory facilities.

M2: To encourage innovation, research culture and team work among students.

M3: Interact and work closely with industries and research organizations to accomplish knowledge at par.

M4: To train the students for attaining leadership with ethical values in developing and applying technology for the betterment of society and sustaining the global environment.

Program Educational Objectives (PEOs)

The Graduates, after a few years of Graduation will be able to:

I. **Apply** the latest in-depth knowledge in the field of Electronics and Communication Engineering with Mathematical applications to address real life challenges.
II. **Exhibit** the confidence for independent working and / or spirit to work cohesively with group.
III. **Readily** be accepted by the Industry globally.
IV. **Develop** design skills, fault diagnosis skills, communication skills and create research orientation.
V. **Inculcate** professional, social ethics and to possess awareness regarding societal responsibility, moral and safety related issues

Programme Outcomes (POs):

Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)

13. Design economically and technically sound analog and / or digital systems based on the principles of signal processing, VLSI and communication Engineering (PO-13)

14. Integrate hardware – software, and apply programming practices to realize the solutions in electronics domain. (PO-14)

Scheme and Syllabus

III Semester

Course Code	Course Category	Course Title	Teaching		Examination				
					CIE	Theory (SEE)		Practical (SEE)	
			L-T-P (Hrs/Week)	Credits	Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration in Hrs.
18UMAC300	BS	Engg. Mathematics-III	3 - 0 - 0	3	50	100	3	-	-
18UECC300	PC	Electromagnetic Theory	3 - 2 - 0	4	50	100	3	-	-
18UECC301	PC	Digital Circuit Design	3 - 0 - 0	3	50	100	3	-	-
18UECC302	PC	Network Analysis	3 - 2 - 0	4	50	100	3	-	-
18UECC303	PC	Analog Electronic Devices and Circuits	4 - 0 - 0	4	50	100	3	--	--
18UECC304	PC	Signals & Systems	3 - 0 - 0	3	50	100	3	--	--
18UECL305	PC	Analog Electronic Devices and Circuits Laboratory	0 - 0 - 3	1.5	50	--	--	50	3
18UECL306	PC	Digital Circuit Design Laboratory	0 - 0 -3	1.5	50	--	--	50	3
	Total		**19 - 4 - 6**	**24**	**400**	**600**		**100**	

BS- Basic Science, PC- Program Core

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

*SEE for theory courses is conducted for 100 marks and reduced to 50 marks

IV Semester

Course Code	Course Category	Course Title	Teaching		Examination				
			L-T-P (Hrs/Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
					Max. Marks	*Max. Marks	Duration in Hrs.	Max. Marks	Duration in Hrs.
18UMAC400	BS	Engg. Mathematics-IV	3 - 0 - 0	3	50	100	3	-	-
18UECC400	PC	Communication Systems - I	4 - 0 - 0	4	50	100	3	-	-
18UECC401	PC	Control Systems	3 - 2 - 0	4	50	100	3	-	-
18UECC402	PC	Microcontroller	3 - 2 - 0	4	50	100	3	-	-
18UECC403	PC	HDL Programming Using Verilog	3 - 0 - 0	3	50	100	3	--	--
18UECC404	PC	Linear ICs and Applications	3 - 0 - 0	3	50	100	3	--	--
18UECL405	PC	HDL Programming Laboratory	0 - 0 - 3	1.5	50	--	--	50	3
18UECL406	PC	Linear Integrated Circuits Laboratory	0 - 0 -3	1.5	50	--	--	50	3
18UECL407	PC	Introductory Project	0 – 0 - 2	1	50	--	--	--	--
	Total		**19 - 4 - 8**	**25**	**450**	**600**		**100**	

BS- Basic Science, PC- Program Core

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

*SEE for theory courses is conducted for 100 marks and reduced to 50 marks

18UECC300	Electromagnetic Theory	(3-2-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the theory and applications of electromagnetic fields. The course concentrates on the study, interpretation and applications of Coulomb's Laws, Gauss's Law, Poisson's and Laplace's equations, Maxwell's equations in the study of electromagnetic fields in different media.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1-12)/ PSOs (13,14)		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the significance of vectors and solve problems in various co-ordinate systems.	1	-	2,13
CO-2	**Derive** the expression for electric field due to various types of charge distributions using coulomb's Law, gauss's Law and **apply** divergence and curl for studying nature of electric fields.	-	1,2	13
CO-3	**Define** energy and potential and analyze the properties of current flow through conductors and dielectrics using Poisson's and Laplace's equations.	2	1	3,13
CO-4	**Discuss** the concepts and laws governing the steady magnetic fields.	-	1	2,13
CO-5	**Apply** Maxwell's Equations in understanding wave propagation theory	1,2	-	4,13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.4	2.0	1	1	-	-	-	-	-	-	-	-	1	-

Pre-requisites: Basics of Electronics and Electrical Engineering, Integration, Differentiation and Vector algebra.

Contents:

Unit-I

Vector Analysis: Vector Algebra, Rectangular Coordinate system, Vector Field, Dot Product and Cross-Product of vectors, Cylindrical and Spherical coordinate systems.

Coulomb's law and Electric field intensity: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge, line charge and sheet charge distribution. **08L+02T Hrs**

Unit-II

Electric flux density, Gauss' law and Divergence: Electric flux density, Gauss' law, Applications of Gauss' law, Divergence and Divergence theorem.

Energy and potential : Energy expended in moving a point charge in an electric field, Line integral, Definition of potential difference and Potential, Potential field of a point charge and system of charges, conservative property, Potential gradient, Energy density in an electrostatic field. **10L+02T Hrs**

Unit-III

Conductors, Dielectrics and Capacitance: Current and current density, Continuity of current, metallic conductors, Conductor properties and boundary conditions, Boundary conditions for perfect dielectric, capacitance and examples.

Poisson's and Laplace's equations: Derivation of Poisson's and Laplace's equation, Uniqueness theorem, Examples of solutions of Laplace's and Poisson's equations. **08L+02T Hrs**

Unit-IV

The steady magnetic field: Biot-Savart law, Ampere's circuital law, Curl and the Stokes Theorem, magnetic flux and flux density, Scalar and vector magnetic potentials.

Magnetic Forces and Boundary Conditions: Force on a moving charge and differential current element, Force between differential current elements, Magnetic boundary conditions. **08L+02T Hrs**

Unit-V

Time varying fields and Maxwell's equations: Faraday's law, displacement current, Maxwell's equation in point and integral form.

Wave Propagation: Wave Propagation in free space and dielectrics.

08L+02T Hrs

Reference Books:

1) Hayt & Buck, "Engineering Electromagnetics", Tata McGraw-Hill, 7th edition, 2006.
2) Hayt & Buck, "Engineering Electromagnetics", Tata McGraw-Hill, 8th edition, 2010.
3) Kraus & Fleisch, "Electromagnetics with Applications", McGraw Hill, 5th edition, 1999.

4) Edminister, “Electromagnetics”, Schaum Outline Series, McGraw Hill, 2nd edition, 2006.

18UECC301 Digital Circuit Design (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on study of various simplification techniques of Boolean expressions and designing of optimized combinational circuits and sequential circuits. It also focuses on application of Digital circuits.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Apply** various techniques to simplify Boolean expressions.	-	2,3	12
CO-2	**Design** combinational circuits using MSI components.	-	2,3	13
CO-3	**Analyze** and **design** combinational circuits using PLDs.	3	-	12
CO-4	**Realize** flip flops and its applications.	3	13	-
CO-5	**Design** of synchronous sequential networks.	-	13	12

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	-	2	2.5	-	-	-	-	-	-	-	-	1	1.67	-

Contents:

Unit-I

Boolean algebra: Canonical forms, prime implicants and irredundant disjunctive expressions prime implicates and irredundant conjunctive expressions. Simplification of Boolean expressions: Karnaugh maps, Quine-McClusky, map entered Karnaugh maps techniques. **08 Hrs**

Unit-II

Logic Design with MSI Components: Binary adders and subtractors, decimal adders, comparators, encoders, decoders, multiplexers and de-multiplexers. Design of combinational circuits using decoders and multiplexers. **08 Hrs**

Unit-III

Programmable logic devices: Introduction, programmable read only memory, programmable logic array, programmable array logic, gate performance considerations, transistor transistor logic, wired logic. **07 Hrs**

Unit-IV

Flip–flops and its applications: Latches, S-R flip flop, J-K flip flop, D and T flip flop, Master-slave flip-flops, edge triggered flip-flops, registers, counters: asynchronous counters, design of synchronous counters: MOD counters, up/down counters, self-correcting counter. **09 Hrs**

Unit-V

Synchronous sequential networks: Structure and operation of clocked synchronous sequential networks, analysis of synchronous sequential networks, serial binary adder as a Mealy/Moore network, sequence recognizer. **07 Hrs**

Reference Books:

1) Donald D Givone, "Digital Principles and Design", Tata McGraw Hill Edition, 2002.
2) John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2001.
3) Charles H Roth Jr; "Fundamentals of logic design", Thomson Learning, 2004.
4) Mono and Kim, "Logic and computer design Fundamentals", Pearson, 2nd edition 2001.

18UECC302	Network Analysis	(3-2-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on mesh and nodal techniques, network theorems and topology, responses of RLC network, AC networks and two port network parameters.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Determine** currents and voltages using mesh / nodal analysis	-	2	1
CO-2	**Solve** network problems by applying various network theorems to reduce	2	5	1

	circuit complexities			
CO3	**Calculate** current and voltages for the given circuit under transient conditions	2	1	-
CO-4	**Apply** various analysis and simplification techniques for AC networks	2	1	13
CO-5	**Solve** for currents and voltages using the concept of network equilibrium equations and **Determine** the various parameters of two port networks.	2,3	1,13	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.6	2.8	3	-	2	-	-	-	-	-	-	-	1.5	-

Pre-requisites: Engineering Mathematics, Basic Electrical Engineering

Contents:

Unit-I

Basic Nodal and Mesh Analysis: Node analysis, Supernode, Mesh Analysis, Supermesh, Nodal Vs Mesh analysis.

Network Theorems: Linearity, Superposition, Source Transformations, Thevenin and Norton equivalent circuits, Maximum power transfer, Millman's, Reciprocity, Tellegen's, Delta-Wye and Wye-Delta conversions. **10L+02T Hrs**

Unit-II

Basic RL and RC circuits : Source-free RL circuit, Properties of exponential response, Source-free RC circuit, General perspective, Unit-step function, Driven RL circuits, Natural and forced response, Driven RC circuits, Source-free parallel circuits. **08L+02T Hrs**

Unit-III

Basic RLC circuits: Source-free series RLC circuits, complete response of RLC circuit.

Circuit analysis in frequency domain : Sinusoidal response, Passive circuit elements in frequency domain, *Kirchhoff's* laws in frequency domain, Series, Parallel and delta-to-Y simplifications, Source transformations & Thevenin-Norton equivalent circuits, Node-voltage method, Mesh-current method**.** **08L+02T Hrs**

Unit-IV

Laplace transforms: Review of Laplace transforms, Nodal and mesh analysis in s-domain.

Frequency Response: Series resonance: Impedance, Phase angle variations with frequency, Voltage and current variation with frequency, Bandwidth, Selectivity, Parallel resonance: Resonant frequency and admittance variation with frequency, Bandwidth and selectivity. **08L+02T Hrs**

Unit-V

Network Topology: Graph of a network, Concept of tree and co-tree, Incidence matrix, Tie-set and cut-set schedules, Branch voltage and current equations, Examples on network equilibrium equations.

Two-Port Networks: Admittance parameters, Impedance parameters, Hybrid parameters, Transmission parameters**,** Interrelationship between parameters.

08L+02T Hrs

Reference Books:

1) William H Hayt. Jr., Jack E Kemmerly, Steven M Durbin, "Engineering Circuit Analysis", Sixth Edition, Tata-McGraw Hill, 2006.
2) Roy Choudhury, "Networks and Systems", Second Edition, New age International Publications, 2010.
3) James W. Nilsson, Susan A. Riedel, "Electric Circuits", Eighth Edition, Pearson Edu. 2008.
4) John D Ryder, "Networks, Lines and Fields", Second Edition, Prentice-Hall of India, 2005.

18UECC303	Analog Electronic Devices and Circuits	(4- 0- 0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on the understanding of electrical characteristics, working and applications of analog electronic devices and the design/analysis of various analog electronic circuits.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design** and **analyze** various wave shaping circuits using Diodes.	1,2	3	-

CO-2	**Discuss** the working, electrical characteristics and biasing techniques for an FET	-	1,2	13
CO-3	**Perform** small signal analysis of FET.	1,2	4	-
CO-4	**Explain** the working of different analog electronic devices and their applications.	-	1,3,4	-
CO-5	**Analyze** the various characteristics of feedback mechanism in amplifiers and oscillators.	1,2,3	-	4,5

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.6	2.8	2.3	1.7	1	-	-	-	-	-	-	-	1	-

Pre-requisites: Basic Semiconductor Physics, Basic Electronics

Contents:

Unit-I

Wave Shaping Circuits using Diodes: Clippers, Clampers.

Field-Effect Transistors: Introduction, construction and working of JFET, transfer characteristics, depletion type MOSFET and enhancement type MOSFET, Introduction to CMOS. **10 Hrs**

Unit-II

FET biasing: Fixed bias, self-bias, voltage divider bias, biasing in Depletion type MOSFETs and Enhancement type MOSFETs.

Small signal analysis of FET: JFET small signal model, small signal analysis of JFET based fixed bias, self-bias, voltage divider bias and source follower configurations, small signal models of depletion type MOSFETs and enhancement type MOSFETs, low frequency response of FET Amplifiers. **12 Hrs**

Unit-III

Feedback amplifiers: Feedback concept, feedback connection types, effect of negative feedback on gain and bandwidth.

Oscillator circuits: Oscillator operation, FET based phase-shift oscillator, Wein Bridge oscillator, Tuned oscillator circuits: FET Colpitts oscillator, FET Hartley oscillator, Crystal oscillator. **10 Hrs**

Unit-IV

Other Two terminal Devices: Light emitting diode (LED), Liquid crystal displays (LCD), Photo conductive cell, Photo diode and Solar cell, Phototransistors, Schottky barrier diodes, Varactor diodes, Power diodes, Tunnel diodes, IR Emitters, Thermistors. **10 Hrs**

Unit-V

Thyristors: Introduction, construction, working and characteristics of SCR, TRIAC, UJT.

Power amplifiers: Introduction, classification of power amplifiers, series fed and transformer coupled Class A, Class B amplifier circuits: Push Pull operation, Class C and Class D amplifier circuits, Amplifier distortion and heat sink. **10 Hrs**

Reference Books:

1) Robert L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuit Theory”, 10/e, PHI, 2012.
2) Jacob Millman and Christos C. Halkias, - “Integrated Electronics”, 8/e, McGraw Hill, 1999.
3) D. A. Bell, “Electronic Devices & Circuits”, 4th Edition, PHI, 2007.
4) M. H. Rashid, “Power Electronics”, Pearson Education 3rd Edition, 2009.

18UECC304 Signals & Systems (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on learning mathematical model for a signal, properties of a signals and systems, representation of a signal in different domains. Also, the course emphasizes on relation between Fourier representations, sampling and reconstruction of a signal.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1-12)/ PSOs (13,14)		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** different types of signals, systems and its properties.	1	2	

CO-2	**Analyze** the time domain signals and **Solve** for the system response.	1,2		13
CO-3	**Analyze** the frequency domain signals	1	2	
CO-4	**Relate** different Fourier representations and **apply** it for various applications**.**	1	2	3, 13
CO-5	**Apply** the Z- transform to analyze discrete-time signals and systems.	1	2	

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	3	2.2	1	-	-	-	-	-	-	-	-	-	1	-

Pre-requisites: Calculus

Contents:

Unit-I

Introduction: Definitions of signals and systems, Classification of signals, Basic operations on signals, Elementary signals, Properties of systems. **07 Hrs**

Unit-II

Time Domain Representation: Convolution, Interconnection of LTI systems, Relations between LTI system properties and impulse Response, Solving Differential and Difference Equations, Block diagram representation. **08 Hrs**

Unit-III

Frequency domain Representation: Complex Sinusoids and Frequency response of LTI Systems, Fourier Representations for four classes of signals - DTFS, FS, DTFT, FT. **08 Hrs**

Unit-IV

Frequency domain Representation: Properties of Fourier transform, Frequency response of LTI systems.

Applications of Fourier Representations: Relating FT to FS, DTFT to DTFS, FT to DTFT, FT to DTFS, convolution and multiplication with mixtures of periodic and non-periodic signals, sampling and reconstruction of continuous time signals. **08 Hrs**

Unit-V

Z–Transforms: Basic concepts, Properties of region of Convergence, Properties of the z-transform, Inversion of z-transform: Partial fraction expansion method and power series method, Unilateral z–transform, Transfer function. **08 Hrs**

Reference Books:

1) Simon Haykin, Barry Van Veen, “Signals and Systems”, 2/e, Wiley Publications, reprint 2009.
2) Alan V Oppenheim, Alan S, Willsky and A Hami Nawab**,** “Signals and Systems”, Pearson Education Asia / PHI, 2/e, 1997. Indian Reprint 2002.
3) H. P Hsu and R. Ranjan, “Signals and Systems”, Schaum’s outlines, TMH, 2006.
4) Luis F. Chaparro, Aydin Akan, "Signals and Systems Using MATLAB", 3/e, Academic Press, 2019.

18UECL305 Analog Electronic Devices and Circuits Laboratory (0-0-3)1.5

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on conducting experiments to determine characteristics, understand the working and applications of analog electronic devices and circuits.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1-12)/ PSOs (13,14)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	**Conduct** experiments to determine characteristics of analog electronic devices such as BJTs and FETs.	1	3	5,13
CO-2	**Design** and **Analyze** the wave shaping circuits using diodes.	1,2	3	13
CO-3	**Design** and **Analyze** RC coupled amplifier.	1,2	3	13
CO-4	**Demonstrate** the working of oscillator circuits.	3	1,2	13
CO-5	**Design** and **Analyze** Power amplifiers.	1,3	5	13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.8	2.66	2.4	-	1.33	-	-	-	-	-	-	-	1	-

List of Experiments:

1) Full Wave Rectifier Circuit Operation (with and without filter).
2) Clipping Circuits using Diodes.
3) Clamping Circuits using Diodes.
4) Bipolar Junction Transistor (BJT) Characteristics.
5) Single stage RC Coupled (CE) Amplifier.
6) RC Phase Shift Oscillator using FET.
7) Hartley Oscillator using FET.
8) Colpitts Oscillator using FET.
9) Junction Field Effect Transistor (JFET) Characteristics.
10) Complementary Symmetry class B push-pull power amplifier.
11) Transistor as a switch/ Relay driver

Reference Books:

1) Robert L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuit Theory”, 10/e, PHI, 2012.
2) Jacob Millman and Christos C. Halkias, - “Integrated Electronics”, 8/e, McGraw Hill, 1999.
3) D. A. Bell, “Electronic Devices & Circuits”, 4th Edition, PHI, 2007.
4) M. H. Rashid, “Power Electronics”, Pearson Education 3rd Edition, 2009.

18UECL306	Digital Circuit Design Laboratory	(0-0-3) 1.5

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on design and implementation of optimized combinational and sequential circuits.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Design** and **realize** the digital circuits for given Boolean equations.	2	13	12
CO-2	**Design** and **implement** arithmetic circuits, encoder, decoder ,multiplexer and other	2,3	13	-

	combinational circuits.			
CO-3	**Implementation** of code converters and **realization of** flip flops.	2	3,13	-
CO-4	**Design** and **implement** sequential circuits**.**	2,3	13	-
CO-5	**Realize** shift registers.	2	3	13

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	-	3	2.5	-	-	-	-	-	-	-	-	1	1.8	-

List of Experiments:

1) Realization of adder / subtractor using basic gates and universal gates.
2) i) Code conversion using logic gates.
   ii) Realization of parallel adder and parallel subtractor / BCD to excess-3 converter and vice-versa using IC 7483.
3) i) Design and implementation of comparator using logic gates.
   ii) Implementation of comparator using 7485 IC.
4) i) Realization of MUX using universal gates.
   ii) Realization of DEMUX using universal gates.
5) i) Implementation of the given function using MUX IC 74153.
   ii) Design and implementation of adders and subtractors using decoder IC 74139.
6) i) Verification of priority encoder IC 74148.
   ii) Use of BCD to seven segment decoder IC 7447 to drive the LED display.
7) i) Verification of flip-flops using logic gates and IC's.
   ii) Conversion of flip-flops.
8) Realization using IC 7476
   i) Ring counter
   ii) Johnson Counter
9) Design and implementation of synchronous counters.
10) Design and implementation of asynchronous counters.

Reference Books:

1) Donald D Givone, "Digital Principles and Design", Tata McGraw Hill Edition, 2002.
2) John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2001.
3) Charles H Roth, Jr; "Fundamentals of logic design", Thomson Learning, 2004.
4) Mono and Kim, "Logic and computer design Fundamentals", Pearson, 2nd edition 2001.

IV Semester

18UECC400	Communication Systems - I	(4-0-0)4

Contact Hours: 52

Course Learning Objectives (CLOs):

The course focuses on time and frequency domain description of various analog modulation techniques, their generation and detection with necessary mathematical analysis. Various types of noise and performance of radio receivers in the presence of noise is covered in the course. The course also deals with theoretical bounds on sampling rates, practical aspects of sampling, quantization and various encoding methods.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** various analog modulation techniques in time and frequency domain	1,2		
CO-2	**Describe** the generation and detection of various analog modulation techniques		1,3,13	12
CO-3	**Explain** various types of noise and **evaluate** the performance of the receiver in presence of noise		1,2,3	
CO-4	**Derive** sampling rates to convert signal from analog to digital and practical aspects of sampling	1,2	3	
CO-5	**Describe** types of quantization and various source encoding techniques for data transmission		1,2,3,13	12

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.4	2.5	2	-	-	-	-	-	-	-	-	1	2	-

Pre-requisites: Fourier analysis, Analog Electronic Circuits.

Contents:

Unit-I

Amplitude Modulation: Introduction to communication system, Need for modulation, AM, DSBSC, SSB, VSB: time domain description, frequency domain description, modulation index, bandwidth, power relations, modulation by several sine waves, generation, detection, quadrature carrier multiplexing, comparison of various amplitude modulation techniques, frequency translation, frequency division multiplexing, applications: AM radio. **12 Hrs**

Unit-II

Angle Modulation: Frequency modulation, Phase modulation, time domain description, spectrum analysis of FM waves, transmission bandwidth, narrow band FM, wideband FM, generation of FM waves: indirect FM, direct FM, demodulation: balanced frequency discriminator, zero crossing detector, phase locked loop, applications: FM radio, FM stereo multiplexing. **09 Hrs**

Unit-III

Noise in CW Modulation systems: Introduction, various types of noise, narrow band noise, noisy receiver model, noise in DSB-SC receivers, noise in SSB receivers, noise in AM receivers, noise in FM receivers, pre-emphasis and de-emphasis in FM **09 Hrs**

Unit-IV

Sampling Process: Introduction, sampling theorem, signal distortion in sampling, practical aspects of sampling: natural sampling, flat top sampling, sample and hold circuit, time division multiplexing, T1 carrier multiplexing, pulse modulation techniques: PAM, PWM, PPM **12 Hrs**

Unit-V

Waveform Coding Techniques: Quantization, quantization noise, signal to quantization noise ratio, robust quantization, Pulse Code Modulation, Differential Pulse Code Modulation, Delta Modulation, Adaptive Delta Modulation. **10 Hrs**

Reference Books:

1) Simon Haykin, "An introduction to analog and digital communications", John Wiley India Pvt. Ltd., 2008.
2) Simon Haykin, "Communication systems", 5/e, John Wiley India Pvt. Ltd., 2009.
3) Simon Haykin, "Digital Communications", John Wiley India Pvt. Ltd., 2009.
4) B. P. Lathi, "Modern digital and analog communication systems", Oxford University Press, 4/e, 2010.

18UECC401	Control Systems	(3-2-0) 4

Contact Hours: 52 Hrs

Course Learning Objectives (CLOs):

The course focuses on mathematical modeling, arriving at system transfer function from block diagram / signal flow graph, finding out time and frequency response of the control systems, various methods of finding out stability of a system, state model representation and its solution for electrical systems. Numerical examples are taken up for discussing these topics.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1,12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Classify** different Control Systems with examples and **Analyze** electromechanical systems by mathematical modeling.	1	2	-
CO-2	**Develop** transfer function of a control system using Block diagram reduction technique and signal flow graph method.	1,2	-	-
CO-3	**Determine** Transient and Steady State behavior of systems using standard test signals and it's time response specifications.	1,2	-	13
CO-4	**Analyze and investigate** the stability of different control systems using graphical and mathematical techniques in time domain and frequency domain.	2	13	3
CO-5	**Realization** of basic Compensators and **Understand** the modeling of linear-time-invariant systems using state-space representation.	-	1,2	13

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	2.7	2.6	1	-	-	-	-	-	-	-	-	-	1.3	-

Pre-requisites:
Laplace Transform, Partial Fractions, Differentiation & Integration

Contents:

Unit-I

Modeling of Systems: The control system, Mathematical models of Physical systems: Differential equations of physical systems - Mechanical systems, Translational systems, Rotational systems, Electrical systems, Analogous systems.

Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs. **10L+02T Hrs**

Unit-II

Time Response of feedback control systems: Standard test signals, Unit step response of First and second order systems, Time response specifications, Steady-State Errors and Error Constants, Types of Control Systems, Dominant Poles of Transfer Functions.

Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh-stability criterion, Relative stability analysis. **08L+02T Hrs**

Unit-III

Root-Locus Techniques: Introduction, the root locus concepts, Construction of root loci, numerical examples.

Stability in the frequency domain: Mathematical preliminaries, Nyquist Stability criterion, Assessment of relative stability using Nyquist criterion, numerical examples. **08L+02T Hrs**

Unit-IV

Frequency response analysis: Introduction, Correlation between time and frequency response, Bode plots, All pass and minimum phase systems, Experimental determination of transfer functions. **08L+02T Hrs**

Unit-V

Compensation: Introduction, Types of compensators, Realization of basic compensators.

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations, Transfer Function from the State Model. **08L+02T Hrs**

Reference Books:

1) I.J.Nagarath and M.Gopal, "Control Systems Engineering", 5/e, New Age International (P) Limited, Publishers, 2007.
2) A. Anand Kumar, "Control Systems", PHI, 2013.
3) K. Ogata, "Modern Control Engineering", 4/e, Pearson Education Asia/PHI, 2002.
4) B. C. Kuo, "Automatic Control Systems", 7/e, EEE, PHI, 2005.
5) A.K. Jairath, "Solutions and Problems of Control Systems", 2/e, CBS Publishers & Distributors, 1997.

18UECC402	Microcontrollers	(3-2-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

This course focuses on architectural features and instruction set of 8051 microcontroller. It also focuses on programming using assembly language of 8051 and C language, programming the timers in different modes, programming for serial communication, interrupts and interfacing devices.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the architectural features of microcontrollers 8051.	-	14	1
CO-2	**Explain** the operations of data movement, logical and arithmetic instructions.	-	1,14	-
CO-3	**Write** programs on branch instructions in assembly Language.	2,3,4	13,14	-
CO-4	**Program** the timers in different modes using assembly and C programming and for serial communication between 8051 and peripherals.	-	2,3,14	-
CO-5	**Analyze and Implement** a program for 8051 interrupts and other peripherals.	3,4	1,14	-

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.66	2.5	2.66	3	-	-	-	-	-	-	-	-	2	2

Pre-requisites: Digital Circuits and basic programming skills.

Contents:

Unit-I

Microprocessors and Microcontrollers: Introduction, Overview of 8085 Microprocessor, difference between Microprocessors and Microcontrollers, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture. The 8051 Architecture-Block diagram, Pin Configuration, 8051 port structure. **8L+2T Hrs**

Unit-II

Addressing Modes and Operations: Introduction, Addressing modes, External data transfer, Code Memory, Read Only Data transfer / Indexed Addressing modes, PUSH and POP opcodes, Data exchanges, Example Programs; Byte level logical Operations, Bit level Logical Operations, Rotate and Swap Operations, Example Programs. Arithmetic Operations: Flags, Incrementing and Decrementing, Addition, Subtraction, Multiplication and Division, Example-programs. **8L+2T Hrs**

Unit-III

Jump and Call Instructions: The JUMP and CALL Program range, Jumps, calls and Subroutines, Interrupts and Returns, Examples.

8051 programming in C: Data types and time delays in C for 8051, I/O programming, logic operations, data conversion programs. **08 Hrs**

Unit-IV

Timer/Counter Programming in 8051: Programming 8051 Timers, Counter Programming, programming timers 0 and 1 in C and ALP.

8051 Serial Communication: Basics of Serial Communication, 8051 connections to RS-232, 8051 Serial communication Programming, Serial port programming in C and ALP. **10L+2T Hrs**

Unit-V

Interrupts Programming: 8051 Interrupts, Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Interrupt Priority in the 8051, interrupt programming in C and ALP

Embedded Sub Systems Using 8051: Interfacing 8051 to LCD, Keyboard, DAC and Stepper Motor. **10L+2T Hrs**

Reference Books:

1) Kenneth J. Ayala, "The 8051 Microcontroller Architecture, Programming and Applications", 3rd Edition, Cengage Learning, 2011.
2) Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay, "The 8051 Microcontroller and Embedded Systems – using assembly and C", 2nd Edition, Pearson, 2008.
3) Predko, "Programming and Customizing the 8051 Microcontroller", TMH, 2005.
4) Dr. Ramani Kalpathi and Ganesh Raja, "Microcontroller and its applications", Sanguine Technical Publishers, 2005.

18UECC403	HDL Programming using Verilog	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on HDL programming concepts, Verilog constructs, and application to the implementation of various digital circuits. Also, course focuses on hardware description of a digital system using Verilog.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Recognize** the need for HDL and **describe** typical design flow and design methodologies of VLSI.	-	3	1
CO-2	**Identify** and **illustrate** various terminologies, data types and system tasks of verilog language.	-	2, 14	-
CO-3	**Apply** the knowledge of various design models and techniques in verilog programming to describe the digital system.	-	1,4,13, 14	2,3
CO-4	**Analyze** the given task and **develop** the program using subroutines.	-	14	2,3,4
CO-5	**Identify** the useful modeling techniques in verilog and **illustrate** the concept of synthesis, mapping and optimization	-	2,14	1,3,4

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.33	1.5	1.25	1.33	-	-	-	-	-	-	-	-	2	2

Pre-requisites: Digital circuit design, Programming fundamentals

Contents:

Unit-I

Overview of Digital Design with Verilog HDL: Typical VLSI Design Flow, Design Méthodologies, 4 bit Ripple Carry Counter, Modules, Instances, Components of a Simulation, Examples.

Basic Concepts & Modules and Ports: Basic Concepts: Lexical Conventions, Data types, System Tasks and Compiler Directives, Modules, Ports, Examples.

09 Hrs

Unit-II

Gate Level Modeling: Gate types And/ Or gates, Buffer / Not gates, Example, Gate Delays, Rise, Fall and turn –off delays, Minimum / Typical /Maximum values.

Dataflow Modeling: Continuous Assignments, Delays, Expressions, Operations, and Operands, Operator types, Examples. **08 Hrs**

Unit-III

Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multi-way Branching, Loops, Traffic light controller, Examples. **08 Hrs**

Unit-IV

Tasks and Functions : Difference between Tasks and Function, Tasks declaration and invocation, Task examples, Function declaration and invocation, Function examples. **07 Hrs**

Unit-V

Useful modeling techniques: Time Scales, Useful System tasks.

Logic Synthesis with Verilog HDL : Logic Synthesis, Synthesis information from module inputs / Outputs, Synthesis Design Flow, RTL Description, translation, Logic Optimization, Technology Mapping and Optimization, examples. **07 Hrs**

Reference Books:

1) Samir Palnitkar, "Verilog HDL", 2/e, Pearson Education, IEEE 1364-2001 Compliant, 2015.
2) T.R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", ISBN: 978-0-471-44148-9, Wiley-IEEE Press, 2004.
3) Nazeih M Botros, "HDL Programming, VHDL and Verilog", Deamtech Press, 2007.
4) Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using verilog", Elsevier, 2010.

18UECC404	**Linear ICs and Applications**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on understanding fundamentals of Op-amp ICs, analysis of its performance and responses in various circuit configurations and its various applications. It also focuses on other linear ICs such as 555 Timer, PLL and their various applications.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the fundamentals of op-amp and **derive** the expressions for gain and input resistance for differential amplifier.		1	2

CO-2	**Derive** the expressions for gain, bandwidth and resistances of op-amp with negative feedback and **analyze** frequency response.		1,3	2
CO-3	**Design** various circuits using op-amp for different applications and **analyze** their operational characteristics.		13	1,2,3
CO-4	**Design** and **explain** the filters and oscillators using op-amp.	3	13	1
CO-5	**Design** and **explain** comparator and converter circuits, 555 Timer and PLL.		1,2	

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.6	1.25	2										2	

Pre-requisites: Transistor biasing and analysis, Network analysis,

Contents:

Unit-I

Differential Amplifiers: Dual input-Balanced output differential amplifier, Dual input-Unbalanced output differential amplifier, Level translator.

Operational amplifier Fundamentals: Block diagram representation of Op-amp, Op-amp parameters such as Input offset voltage, Input offset current, Input bias current, CMRR, SVRR, Output voltage swing, Output short circuit current, Slew rate and Gain-bandwidth product, The ideal Op-amp, Equivalent circuit of an Op-amp, Ideal voltage transfer curve, Open Loop Op-Amp configurations **07 Hrs**

Unit-II

Op-Amp with Negative Feedback: Block diagram representation of feedback configuration, Voltage series feedback amplifier, Voltage shunt feedback amplifier, Differential Amplifier, Input offset voltage compensation. Op-Amps frequency response: High frequency Op-amp equivalent circuit, Open loop voltage gain as a function of frequency, Closed Loop frequency response. **08 Hrs**

Unit-III

OP-Amp Applications: Peaking amplifier, Summing, scaling and averaging amplifiers, Instrumentation amplifier, Voltage to current converter with floating load, Current to voltage converter, Integrator, Differentiator. **07 Hrs**

Unit-IV

Active filters and Oscillators: Active filters, first and second order low pass and high pass Butterworth filter, Phase shift oscillator, Wein-bridge oscillator, Square and triangular wave generators, voltage controlled oscillators. **08 Hrs**

Unit-V

Comparators and Converters: Basic comparator, Zero crossing detector, Schmitt trigger, A/D and D/A converters, peak detectors, sample and hold circuit. Specialized IC applications: 555 timer-Basic timer circuit, 555 timer used as astable and mono-stable multivibrator, PLL-operating principles, Monolithic phase locked loops, PLL applications. **09 Hrs**

Reference Books:

1) Ramakant A. Gayakwad,"Op-Amps and Linear Integrated Circuits", 3/e, PHI.
2) D. Roy Choudhury and Shail B. Jain,"Linear Integrated Circuits", 3/e, New Age International, Reprint 2006.
3) Robert. F. Coughlin & Fred. F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", 5/e PHI, 2006.
4) William D. Stanley, "Operational Amplifiers With Linear Integrated Circuits",, 4/e, Pearson

18UECL405	**HDL Programming Laboratory**	**(0-0-3) 1.5**

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on experiments based on HDL programming for digital circuit design using Verilog. Also, the course contemplates the interfacing programs to interface different hardware components using Field Programmable Logic Device (FPGA).

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Relate** the need for HDL in Typical design flow of VLSI Technology.	-	14	1
CO-2	**Apply** appropriate techniques, resources, and EDA tools for modeling, simulation and synthesis of various digital systems.	5,14	3,4,13	1,2

CO-3	**Design** combinational and Sequential circuits using various programming techniques.	-	3,4,5,13, 14	1,2
CO-4	**Build** the HDL model to interface FPGA kits with various peripherals	14	5	1,2,3,4
CO-5	**Generate** the test vectors for the HDL model using stimulus block.	-	3,4,5,13, 14	1,2

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1	1	1.75	1.75	2.25	-	-	-	-	-	-	-	2	2.4

List of Experiments:

1) Write a Verilog code to implement the following Basic Gates: (Using Dataflow, Behavioral and Structural style of modelling).
2) Write a Verilog code to implement Adders, Subtractors, Encoders and Decoders. (Using Dataflow, Behavioral and Structural style of modelling).
3) Write a Verilog code to implement Multiplexers, De-multiplexers, Code converters, Comparators.
4) (Using Dataflow, Behavioral and Structural style of modelling).
5) Write a Verilog Code to implement 4-bit ALU. Verify the same generating test vectors for the various operations. Write the test bench (stimulus block) and verify that it behaves as ALU.
6) Design a 4-bit ripple carry adder using concept of hierarchical structured modeling by using module instantiation, tasks and functions.
7) Write the verilog code to implement all flip flops.
    a) Write a Verilog code to implement the following:
    b) 4-bit Shift register (Right shift and left shift)
    c) 4-bit Ring counter and Johnson counter
    d) 4-bit up counter and 4-bit down counter
    e) 4-bit updown counter
    f) Any given sequence counter (4-bit)
    g) BCD updown Counter
    h) Mealy and Moore’s synchronous circuit design.
8) Write a verilog code to run the stepper motor in clockwise and anti-clockwise direction.
9) Write a verilog code to generate any given waveforms using DAC kit.
10) Write a verilog code to Interface hex keypad and display it on 7-segment LED.

Note: Simulation should be done using Xilinx ISE tool and Implementation on Spartan –6 FPGA Kits.

Reference Books:

1) Samir Palnitkar, "Verilog HDL", 2/e, Pearson Education, IEEE 1364-2001 Compliant, 2015.
2) T.R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", ISBN: 978-0-471-44148-9, Wiley-IEEE Press, 2004.
3) Nazeih M Botros, "HDL Programming, VHDL and Verilog", Deamtech Press, 2007.
4) Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using verilog", Elsevier, 2010.

18UECL406	**Linear Integrated Circuits Laboratory**	**(0-0-3) 1.5**

Contact Hours: 36

Course Learning Objectives (CLOs):

The course focuses on experiments highlighting various applications of linear ICs: op-amp and 555 timer.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-12)/ PSOs (13,14)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** Op-amp as DC and AC amplifier in inverting and non-inverting configuration			1
CO-2	**Design** Op-amp based circuits for various arithmetic operations, filters and comparators and DAC.	2	3	1
CO-3	**Design** of 555 timer as multivibrator.	2	4	1
CO-4	**Demonstrate** the use of Op amp as wave-shaping and rectifier circuits.		13	1,2
CO-5	**Design** various waveform generators using Op-amp.	13	1,2	

POs/PSOs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Mapping Level	1.25	2.25	2	2									2.5	

List of Experiments:

1) Operational amplifier as voltage follower, inverting and non-inverting amplifier.
2) Operational amplifier for implementing given arithmetic expressions.
3) Instrumentation amplifier using Op-Amps.
4) Design low-pass and high-pass first and second order Butterworth filters.
5) Design a Schmitt Trigger for a given UTP and LTP.
6) Design R-2R DAC using OP-Amp.
7) Design of multivibrators for given specifications using IC-555.
8) Wave shaping Circuits using Op-Amp.
9) Waveform Generators using Op-Amp.
10) Rectifiers using Op-amp.

Reference Books:

1) Ramakant A. Gayakwad,"Op-Amps and Linear Integrated Circuits", 3/e, PHI.
2) D. Roy Choudhury and Shail B. Jain,"Linear Integrated Circuits", 3/e, New Age International, Reprint 2006.
3) Robert. F. Coughlin & Fred. F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", 5/e PHI, 2006.
4) William D. Stanley, "Operational Amplifiers With Linear Integrated Circuits",, 4/e, Pearson

18UECL407	Introductory Project	(0-0-2) 1

Contact Hours: 24

Course Learning Objectives (CLOs):

The course provides an exposure to the students to identify simple societal problems and propose a technical solution. It also helps them to find related material, use appropriate tool to obtain the solution and prepare a report based on the work carried out.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		Mapping to POs(1-12)/ PSOs (13,14)		
		Substantial Level (3)	Moderate Level (2)	Slight Level (1)
CO-1	Conduct a **survey** and **identify** the community needs.	-	6, 7	2
CO-2	**Formulate** the problem statement.	-	2	1
CO-3	**Propose** a solution by applying the fundamental knowledge of basic sciences and basic engineering courses	-	1,2	3

CO-4	**Develop** the team spirit, communication and management skills.	-	9,10,12	11
CO-5	**Prepare** a report and present the findings.	-	9,12	-

POs/PSOs	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Mapping Level	1.5	1.7	1			2	2		2	2	1	2		